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ELECTRICAL CHARACTERIZATION OF SPECIAL PURPOSE LINEAR MICROCIRCUITS

General Electric Ordnance Systems

J. S. Kulpinski, et al

SEP 2 3 1980

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SECURITY CLASSIFICATION OF THIS PAGE(When Date Entered)

Adjustable Negative Voltage Regulators, Precision BiFet Op Amps, Multiple BiFet Op Amps, 12 Bit A/D Converters, 12 Bit D/A Converters, Precision Voltage References, Precision Sample/Hold Amplifiers.

Data obtained during device characterization is published in handbook form obtainable under separate cover from this document. Samples of data sheets, histograms, and plots, are included in this report, however.

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Acronyms and Symbols

```
Ampere
A/D
                      Analog to Digital
ΑE
                      Gain Error
                      Open loop voltage gain (single-ended,
AVS (±)
                           0 \text{ to } +, 0 \text{ to } -)
BPO
                      Bipolar offset
BPOE
                      Bipolar offset error
BW
                      Bandwidth
CM
                      Common mode
CMR
                      Common mode rejection
CPW
                      Clock pulse width
CS
                      Channel Separation
O<sub>T</sub> (n)
                      A/D converter transition voltage - nth transition
D/A
                      Digital to Analog
ďΒ
                      Decibel
DESC
                      Defense Electronics Supply Center
DUT
                      Device Under Test
E (n)
                      A/D converter transition voltage bit error
                           in LSB, with transition
E(n)
                      Static A/D converter transition voltage less
                           transient error contribution in LSBs
\mathbf{E}_{\mathbf{O}}(n)
                      Amplified difference voltage. Difference between
                           reference D/A converter and the DUT output
                           nth transition
FRR
                      Feedthrough Rejection Ratio
FSV
                      Full Scale Voltage
FSVR
                      Full Scale Voltage Range
G
                      Voltage gain
G_{\mathbf{E}}
                      Voltage gain error
GE
                      General Electric Company
GEOS
                      General Electric Company, Ordnance Systems
GND
                      Ground
                      Adjustment pin current
I<sub>adj</sub>
+I<sub>CC</sub>
                      Positive supply current
                      Hold capacitor charging current (+ input)
ICH (+)
                      Hold capacitor charging current (- input)
ICH (-)
I<sub>con t</sub>
                      Control pin current
ICs
                      Integrated Circuits
IHL (+)
                      Leakage current into hold with + charge
                      Leakage current into hold with - charge
IHL (-)
+I<sub>IB</sub>
                      Input bias current, non-inverting input
-IIB
                      Input bias current, inverting input
IIH
                      High level input current
                      Low level input current
IIL
                      Input offset current
IIO
\Delta I_{10}/\Delta T
                      Input offset current/temperature coefficient
```

ILOG	Logic power supply current
I _{OS} (+)	Output short circuit current (for positive output)
Ios (-)	Output short circuit current (for negative output)
IQ	Quiescent current
IREF	Reference voltage supply current
IS	Temperature stabilizer supply current
ISI	Initial temperature stabilizer supply current
JAN	Joint Army Navy
JC-41	JEDEC Committee on Linear Integrated Circuits
JEDEC	Joint Electron Devices Engineering Council
ln	Natural logarithm
LSB	Least significant bit of D/A or A/D converter
LSI	Large Scale Integration
LTPD	Lot Tolerance Percent Defective
mA.	Milliampere
MCE (n)	Major carry error where n = 1 is major transition
	with all bits changing
MCE (n)	Major carry error less transient error contribution
	where $n = 1$ is major transition with all bits
	changing
MPCAG	Military Parts Control Advisory Group
mV	Millivolt
N ₁ (BB)	Broadband noise
N _O	Output noise voltage
N1(PC)	Popcorn noise
OS	(GE) Ordnance Systems
PD	Quiescent power dissipation
pk	Peak
PPM	Parts per million
+PSRR	Power Supply Rejection Ratio, positive supply
PSS	Power Supply Sensitivity
QPL	Qualified Product List
RADC	Rome Air Development Center
R _F	Amplifier feedback resistor
R _T s7н	Amplifier input scanning resistor
S/N	Sample and Hold Circuit Serial Number
SR(+)	
	Slew rate (max ΔV_0 / Δt), positive Ambient temperature
T _A	Acquisition time (S/H)
t _{ac} t _{ap}	Aperture time (S/H)
TR(t _r)	Transient response, rise time
TR(OS)	Transient response, overshoot
ts	Settling time of step response to specified accuracy
t _{SLH}	Settling time, low-to-high
t _{SHL}	Settling time, high-to-low
TŢĹ	Transistor - transistor logic
T ² L	Transistor - transistor logic
VADCIN	A/D converter input voltage
-	

```
Vad i
                       Adjustment pin voltage
V<sub>RE</sub>
                       Base-to-emitter voltage
Vcc
                       Supply voltage
Vcont
                       Control pin voltage
v_{\mathbf{F}}
                       Forced voltage
                       "Hold" step voltage
VHS
                       Logic "1" input voltage
VIH
                       Logic "0" input voltage
VIL
VIN
                       Input voltage
VIO
                       Input offset voltage
                       Adjustment for input offset voltage
VIO ADJ(+)
VOH
                       Output Voltage, high level
                       D/A output voltage on straight line between
<sup>V</sup>0I (n)
                           zero and FS for address n
VOL
                       Output Voltage, low level
V<sub>OM(n)</sub>
                       D/A output voltage measured for address n
V<sub>OP</sub>
                       Output voltage swing (peak)
VOUT
                       Voltage output
VOUT (RECOV)
                       Regulator output recovery voltage after output
                           short to ground
v_R
                       Reference Voltage
V<sub>RDAC</sub>(n)
                       Reference D/A converter output for address n
VR LINE
                       Line regulation
                      Load regulation
VR LOAD
VROS
                       Reference D/A output offset voltage
VRTH
                      Thermal voltage regulation
+Vs
                      Positive supply voltage
<sup>V</sup>START
                      Voltage start-up
Zi
                       Input Impedance
Z<sub>o</sub>
                      Output Impedance
                      Data mean of X
.°C
                      Degrees centigrade
u
                      Micro
uF
                      Microfarad
uV
                      Microvolt
us
                      Microsecond
8
                      Delta
                      Sigma
  + NL
                      Summation of maximum positive bit weight errors
  - NL
                      Summation of maximum negative bit weight errors
\Delta V_{IO} / \Delta T
                      Input offset voltage temperature coefficient
A VIN/ A VOUT
                      Ripple rejection
A VOUT / A VIN
                      Line transient response
                      Load transient response
\Delta V_R / \Delta T
                      Reference voltage temperature coefficient
                      Thermal resistance
```

PREFACE

This report was prepared by General Electric Ordnance Systems, 100 Plastics Avenue, Pittsfield, Massachusetts, for Rome Air Development Center, Griffiss Air Force Base, New York, under contract F30602-78-C-0195. It covers the period Sept. 78 - Sept. 79. Work effort under this contract will continue for the period Sept. 1979 - Sept. 1980, followed by another technical report.

The work on this project was performed by the Electronic Circuits
Engineering Operation and Components Engineering Unit. Project responsibility
was held by Mr. John Kulpinski of Circuit Design Engineering. Key individuals
who made significant contributions to this work effort were Messrs. Theodore
Simonsen, Louis Carrozza, Donald Van Alstyne, Robert Mossman, John Dunn,
Thomas Wetzel, and George Smith. Mr. Thomas Dellecave, RBRM is the Project
Engineer at RADC for this contract.

LINEAR CHARACTERIZATION

List of Sections

SECTION -	TITLE	P AGE NUMBER
ī	Introduction	i – i
11	BiFET, Op Amps, MIL-M-38510/114	i i - i
	non - 'A' parts 'A' parts	
III	Adjustable Positive Regulators, MIL-M-38510/117 and	
	Adjustable Negative Regulators, MIL-M-38510/118	1 1 1 - i
τv	Multiple BiFET Op Amps, MIL-M-38510/119	1V -i
V	A/D Converters, MIL-M-38510/120	V - i
1 V	12 Bit D/A Converters, MIL-M-38510/121	V1-i
VII	Voltage References, MIL-M-38510/124	V i i - i
IIIv	Sample/Hold Circuits, MIL-M-38510/125	V111-i
IX	Voltage Regulators, Negative, MIL-M-38510/115	1X-i

SECTION 1

INTRODUCTION

TABLE OF CONTENTS

	P a ge
Objectives	1-1
Scope of Applied Effort	1-1
Program Status	I-2
Meetings Attended	1-3
Background	1-3
Development of Slash Sheets	1-4
Characterization Data	I - 5

SECTION 1

INTRODUCTION

Objectives

The major objective of this work effort is to characterize certain linear microcircuit devices for inclusion in MH.-M-38910 ("Ceneral specification for Microcircuits") slash sheets.

Generally, "characterization" of a device type includes several related tasks:

- determination of test parameters and limits
- development of test procedures, compatible with automatic test systems
- verification of limits and test circuits via sample device testing/ evaluation.
- generation of detailed burn-in and life test circuits
- preparation of rough draft slash sheets

A secondary objective of this effort is to provide rollow-up support for maintaining existing linear MIL-M-38510 slash sheets to current status, including support to Rome Air Development Center for manufacturer qualitication and related activities.

All of the characterization effort performed is guided by the fundamental objectives of the JAN 38510 program - namely quality, reliability, interchangeability, and standardization.

Scope of Applied Effort

The specific tasks included in this program are the characterization and specification of the following device types/families:

- Adjustable Positive Voltage Regulators, MIL-M-38510/117
- Adjustable Negative Voltage Regulators, MIL-M-38510/118
- Precision BiFET Op Amps, (LF155A etc), MIL-M-38510/114
- Multiple BiFET Op Amps (single, dual, quad), MIL-M-38510/119
- 12-bit A/D Converters, MIL-M-38510/120
- 12-bit D/A Converters, MIL-M-38510/121
- Precision Voltage References, MIL-M-38510/124
- Precision Sample/Holds, MIL-M-38510/125

Additional required tasks included were:

- Assess pending changes to existing slash sheets and recommend appropriate action.
- Support RADC in the evaluation of manufacturer qualification submittals.

- Interface with manufacturers in development of new spees, or changes to existing spees; attend 30-41 Committee and Subcommittee meetings.
- Complete slash sheets not issued at completion of previous contract.

Program Status

The following new slash sheets were developed on this program:

	Commercial Device Type
MIL-M-38510/117, Positive Adjustable Regulators	uA78MG, uA78G, LM117H, LM117K
MIL-M-38510/118, Negative Adjustable Regulators	uA79MG, uA79G, LM137H, LM137K
MIL-M-38510/119, Multiple BiFET Op Amps	TL061, -062, -064, TL071, 072, 074; uA771, -772, 774; LF151, -153, -147
MIL-M-38510/120, 12-Bit A/D Converters	MN 5200-5207, MN5210 - 5217
MIL-M-38510/121, 12-Bit D/A Converters MIL-M-38510/124, Precision Voltage References MIL-M-38510/125, Sample/Hold	AD562, HI562 LM129, LM199 LF198

Three device types were added to an existing slash sheet also:

MIL-M-38510/114, BiFET Op Amps

LF155A, LF156A, LF157A

Commercial Device Tume

Device characterization is essentially complete for the above specifications with the exception of /120 and /125. The A/D specification has been issued in preliminary form; test hardware and software have been developed, and data is expected soon after publication of this report. The Sample/Hold specification and characterization development is in very early stages; a Table I has been prepared, along with test circuits and a partial Table III, awaiting manufacturer comment. All other specifications and characterizations listed above are complete and include a prepared slash sheet, test adapter hardware and software, and automatic/manual test data.

In addition to the above characterizations, follow-up tasks to previous RADC characterizations were also included in the current contract. This effort included the following:

- Complete characterization of BiFET Op Amps, /114, (non-"A" 155 family), including testing of 68 devices, generation of data handbook, and negotiations at JC-41 Op Amp Subcommittee meeting in San José. Two burn-in circuits were evaluated, also. This is reported in Section II of this report.
- Reviewed and assessed proposed changes to parameters and limits for device type 01, (LM109), on /107, Positive Voltage Regulators. Two manufacturers requested changes via JC-41 Committee letter ballot; GE approved the changes with certain qualifications.

- Reviewed and assessed changes to /115, Negative Voltage Regulators; completed investigation of start-up problems observed earlier at GE.
 This item is reported upon in Section
- Completed slash sheet for DACO8, /113, 8-bit D/A Converters; Tables III and IV were added; corrections/comments received from manufacturers were incorporated.
- Errors in /112, Quad Comparators, pointed out by one manufacturer were checked out and corrected at GE.
- A change to the slew rate test circuit for the 118 Op Amp, /101, was analyzed.
- A slash sheet written by NASA, MIL-M-38510/122, High Slew Rate and Wide Band Op Amps, was reviewed and comments were submitted to RADC.

Meetings Attended (GE internal meetings not included)

JC-41 Committee on Linear ICs
Nov. 1, 2, 1978 - Phoenix, AZ
Feb. 27, 28, 1979 - Monterey, CA
June 19, 20, 1979 - Washington, DC

JC-41 Subcommittee Meetings

Feb. 6, 1979	562 D/A Converter	Peabody, MA
Feb. 7, 1979	5200 A/D Converter	Peabody, MA
May 1, 1979	5200 A/D Converter	Pittsfield, MA
May 29, 1979	5200 A/D Converter	Sturbridge, MA
Aug. 14, 1979	CMOS D/A Converters	San Jose, CA
Aug. 15, 1979	Sample/Holds; Voltage	San Jose, CA
	References	

RADC/GE Meetings

Sept. 21, 1979	Contract	Plans	Pittsfield, MA
Feb. 22, 1979	Contract	Status	Pittsfield, MA
May 2, 1979	Contract	Status	Pittsfield, MA
May 22, 1979	Contract	Status	Rome, NY
Aug. 8, 1979	Contract	Status	Pittsfield, MA

Backg round

General Electric began this effort in September of 1978, having previously completed similar characterization and specification contracts in MIL-M-38510 Linears in 1976 and 1977. Philosophies for establishing parameters, limits, and test circuits for conventional devices like op amps, comparators, and regulators had been negotiated with RADC, DESC, and the device manufacturers in meetings of the JC-41 Committee on Linear Integrated Circuits.

This current effort extended past efforts to newer devices in similar generic families, and in addition established new frontiers in the development of automatic tests and specifications for 12-bit data converters. One slash sheet (/120, 12-bit A/D Converters) represents the first hybrid microcircuit to be specified in military JAN linears.

Whereas in 1976 and 1977 the JAN Linear Program has been "catching up" to the state-of-the-art in developing new specs for existing devices, it is now in some cases leading the development. Witness the slash sheet on single, dual, quad BiFET Op Amps, in which devices from three major manufacturers are just becoming available to users, and 3-terminal adjustable regulators where the JAN spec is ready soon after the market introduction.

Although hybrid A/D converters have been around for awhile, monolithics are just reaching that goal, and manufacturers are faced with new challenges for developing suitable automatic tests for high resolution data converters. Even more ambitious tasks are being planned for the near future, with analog LSI (video A/D converters), non-linear companding DACs, and data acquisition devices in the making.

Development of Slash Sheets

A procedure for developing new slash sheets to MIL-M-38510 has evolved through negotiations among all concerned parties. Device selection is influenced by user need, which is determined both by the marketplace and by organized committees, such as the Military Parts Control Group (MPCAG) at DESC, the G12 Solid State EIA Device Committee, and the Microelectronics Project Group of the Electronics Systems Committee of AIA. These recommendations are balanced with manufacturer recommendations obtained via the JC-41 Committee. Devices having high useage, multiple application potential in military systems, proven performance, and two or more sources are given priority. Single-source devices are acceptable, especially for hybrid devices, although multiple sources are preferred. Manufacturers typically recommend devices for slash sheet action in JC-41 Committees, and then chair a JC-41 Subcommittee for preparation of slash sheet parameters, limits, and test circuits.

The industry data sheet forms the basis for the military specification. Typically, such data sheets do not specify all of the necessary parameters over the military temperature range and over the common-mode voltage range. The JC-41 subcommittee, or the device originating company, usually prepares a proposed spec. Ideally, the device manufacturers would like to have these proposed specs incorporated without further consideration. However, RADC and General Electric experiences in this current program have shown that all of the proposed specs have required some rework, and are unsuitable for issuance "as is".

Data provides another base for determining parameters and limits. Devices for test are purchased from distributors, are also obtained from manufacturers via RADC request. In some cases, the industry-donated sample is tested by a single manufacturer on a volunteer basis. The entire sample

is tested further on a Tektronix S3263 Automatic Test System at (a) ordinance Systems Electronic Test Center. Data obtained at -55 C, +25 C, and +125 c ambient is statistically analyzed and reproduced in histogram format. Recommended limits are compared to the statistical sample data. Parameter limits which are grossly inconsistent with the data are readily identified.

Additions, changes, and alternate approaches are discussed at the committee level. Device anomalies are identified in lab bench tests, often using a curve tracer. Failure modes are also identified. User caution notes are added to the specification if it is deemed appropriate.

Burn-in circuits are usually recommended by the manufacturer and evaluated by RADC and/or GEOS on the available test samples. An objective is to minimize the number of external components while stressing the device near its limits.

Device schematics are presently included in MIL-M-38510 slash sheets. A recent JC-41 Committee recommendation is to delete the schematics and to replace them with a block diagram which shows the basic elements of the device, for devices which are very complex (e.g. data converters).

Rough-draft copies of the final slash sheet are prepared at GEOS and are forwarded to RADC for review. DESC distributes copies of this spec to manufacturers and users for final comments. Following assessment of the comments by all concerned parties, DESC prepares and issues the slash sheet

Characterization Data

Data obtained during device characterization is usually published in handbook form separate from this document. Samples of the data sheets, histograms, and plots, are included in this report, however.

SECTION II

Bi-FET OPERATIONAL AMPLIFIERS MIL-M-38510/114

TABLE OF CONTENTS

		Page
2.1	Background and Introduction	1-1
2.2	Description of Device Types	11-2
2.3	Device Characterization	11-6
2.4	Tabulation of Test Data	11-15
2,5	Discussion	II-47
2.6	Conclusions and Recommendations	í í - 57

LIST OF FIGURES

Figure	Tit le	Page
2-1	rypical Bi-FET Op Amp (LF155/156/157)	<u> </u>
2-2	Bi-FET Op Amp With Bias Current Compensation	11-5
2-3	Test Circuit For Static Tests	11-7
2-4	Test Circuit For Transient Response and Slew Rate	11-11
2-5	Test Circuit For Settling Time	11-13
2-6	Bi-FET Op Amp Test Adapter	11-14
2-7	155A Series V _{IO} Histogram	11-19
2-8	Bi-FET Input Bias Current vs. Common Mode Voltage	11-20
2-9	Bi-FET Input Bias Current vs. Common Mode Voltage	11-21
2-10	Bi-FET Input Bias Current vs. Common Mode Voltage	11-22
2-11	Bi-FET Input Bias Current vs. Common Mode Voltage	11-23
2-12	Bi-FET Input Bias Current vs. Temperature	11-24
2-13	Worse Case Input Bias Current vs. Ambient Temperature	11-25
2-14	Offset Voltage vs. Common Mode Voltage	11-26
2-15	Offset Voltage vs. Common Mode Voltage	11-27
2-16	LF155 & LF156 Transient Response	11-28
2-17	LF157 Transient Response	11-29
2-18	LF155 and LF156 Slew Rates	11-30
2-19	LF157 Slew Rate vs Gain	11-31
2-20	LF155 Series Bi-FET Settling Time	11-32
2-21	Open Loop Voltage Gain vs Load	11-33
2-22	LF155 Series Bi-FET Noise Voltage	11-34

TIST OF TABLES

rable -	ritle	Page
2-1	jest fable For Static fests	11-8
2-2	lest lable for Fransient Response and Slew Rate	11-12
2-3	Typical LF155 Op Amp Data Sheet	11-17
2~4	Typical LF155A Op Amp Data Sheet	11-18
2-5	25 C Statistical Summary For LF155 Series Devices	11-35
2-6	-55 C Statistical Summary For LF155 Series Devices	11-36
2-7	125°C Statistical Summary For LF155 Series Devices	I I-37
2-8	25 C Statistical Summary For LF155A Series Devices	11-38
2-9	-55 C Statistical Summary For LF155A Series Devices	11-39
2-10	125°C Statistical Summary For LF155A Series Devices	11-40
2-11	LF155/6/7 Data Distributions	11-41
2-12	LF155/6/7 Supply Current & Slew Rate	11-43
2-13	LF155 Dynamic Data @ 25°C	11-44
2-14	LF156 Dynamic Data @ 25°C	II - 45
2-15	LF157 Dynamic Data @ 25°C	II-46
2-16	Proposed Electrical Performance Characteristics	11-58

SECTION II

Bi-FET OPERATIONAL AMPLIFIERS MIL-M-38510/114

2.1 Background and Introduction

The initial characterization work on Bi-FET Op Amps was described in technical report RADC-TR-78-275. This report covers the completion of the characterization studies on the LF155 series devices and also includes the characterization of the LF155A precision series devices. The relationship between the generic industry and military device types is shown below:

Generic Industry Type	MIL-M-38510/114 Device Type
LF155	01
LF156	02
LF157	03
LF155A	04
LF156A	05
LF157A	06

As the name implies, "Bi-FET" stands for a mixed technology process in which bipolar and field effect transistors are combined on the same monolithic integrated circuit. Standard bipolar processing is used to make most of the circuit elements except for the top gate and channel of the J-FETs, which depend on the ion implantation process. Fabricating with matched input J-FETs which gives rise to low offset voltage and offset voltage drift is the big contribution of the ion implantation process. Obviously the Bi-FET process enables the best features of bi-polar and J-FET transistors to be incorporated into the design of the I.C. op amp.

With J-FET input transistors, the input bias currents are typically under 100 pA. Also, bandwidth and slew rate are not severely compromised by low input bias current as in the case with bipolar transistor front ends having low input bias currents.

A review of linear device applications in military systems as well as a JC-41 Committee priority list were important factors in characterizing and developing a slash sheet for this family of devices. There are seven semiconductor manufacturers making LF155 series Bi-FET op amps.

2.2 Description of Device Types

A typical schematic circuit of a Bi-FET op amp is shown in Figure 2-1. Matched J-FET transistors are used for the differential input gain stage, the input current source loads and the offset adjustment control. The drain outputs of the input P-channel J-FETs feed a differential bipolar transistor stage. Signal conversion from differential to single ended is made at the collector of Q8. Since current sources exist at both the source and drain terminals of the input J-FETs, some mechanism must also exist to deal with the excess common mode current which is sourced from Q1, but not sunk by J10 and J11. Common mode feedback from the differential bipolar stage current source to the source terminals of J1 and J2 solves this problem.

With J-FET input transistors the op amp bias currents + I_{iB} , and - I_{iB} are much smaller than is possible with bipolar transistors. Since these currents are leakage currents, they are temperature sensitive and approximately double for every 10°C increase in temperature. Low noise and good high frequency response are other benefits of the J-FET front end transistors. The single ended output signal from Q8 and its J3 current source load is further amplified by the class B output stage. This output stage is a little unusual in that a J-FET, J5, complements the other bipolar output transistors. Replacing the standard PNP output transistor with a J-FET increases the phase margin of the device and thus enhances the stability of the device for driving high capacitance loads.

Capacitor C2 is the compensation capacitor which establishes the dominant pole from which the open loop voltage gain is "rolled-off". This capacitor therefore affects the unity gain bandwidth and slew rate of the op amp. Another parameter which affects slew rate is the operating current which is available to drive the compensation capacitor. Both the operating current and the compensation capacitor are variables which the IC manufacturers can control in order to achieve a desired speed/power tradeoff. Device types 01, 02 and 03 are basically the same device with different values of compensating capacitance and/or operating current. Consequently, supply current, slew rate and gain bandwidth product are the parameters which are different between the three device types as outlined below:

	Γ	evice :	Гуре	
Parameter	01	02	03*	Units
Supply Current (max)	4	7	7	mA
Slew Rate (min)	2	7.5	30	V/us
Gain Bandwidth (typ) Product	5	12	50	MHz

^{*}Device type 03 is under compensated and is not guaranteed to be stable for closed loop gains under 5 V/V.

There are design differences among the various vendor furnished LF155 series op amps. In order to reduce the effect of temperature on input bias current, one vendor has added a bias current compensation circuit as shown in Figure 2-2.

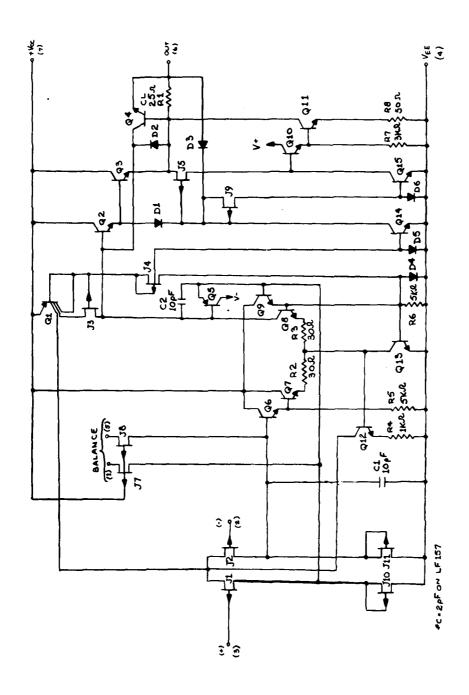


Figure 2-1. Typical Bi-FET OP Amp (LF155/156/157).

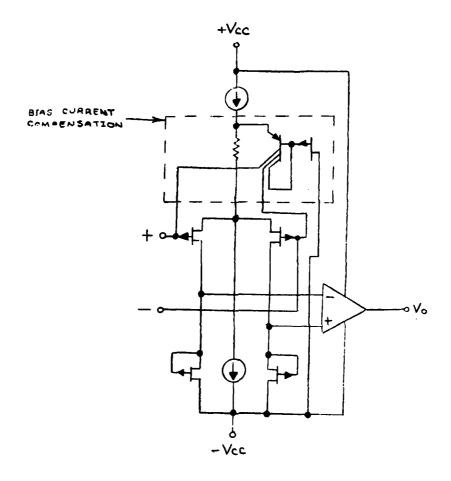


Figure 2-2. Bi-FET Op Amp With Bias Current Compensation.

2.3 Device Characterization

Developing the tests for the Bi-FET op amps was done in a manner similar to previous quad op amp characterization. A test program and an adapter card were developed in order to enable testing with GEOS' Tektronix S-3260 automatic IC test system. While the program and adapter were being developed several devices were analyzed on a Tektronix 577 curve tracer. This manual test phase was good for discovering anomalies and possible automatic tester problems.

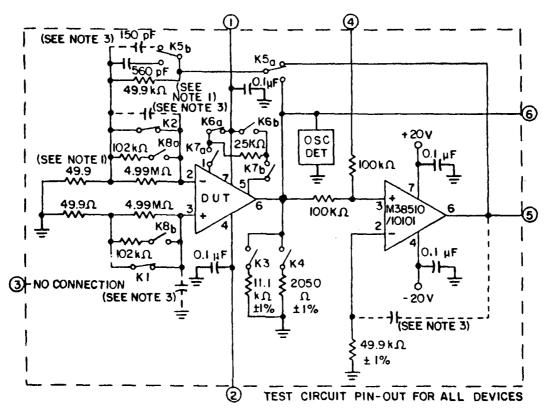
A schematic diagram of the static test circuit is shown in Figure 2-3. All relays are in the normal de-energized position. Operation of the test circuit is straight forward. The device under test (D.U.T) and the nulling amplifier are cascaded within a closed loop gain of 1000. This is done so that millivolts of error voltage with respect to the op amp input are translated into volts D.C. at the nulling amplifier output to the automatic measurement system. The D.U.T. output can be commanded to any voltage in its operating range by applying the negative of the desired voltage to terminal 4. When the non-inverting input to the nulling amplifier is at zero volts, the loop has stabilized and the correct output can be measured. Tests which require the D.U.T. to be exercised over the common mode range are mechanized by swinging the power supplies and commanding the D.U.T. output, while grounding the D.U.T. inputs through 50 ohms. The basic measurement performed by the static test circuit is V_{io} or offset voltage. Most of the other parameters are derived from this basic measurement. A schedule of parameters, test conditions and equations is shown in Table 2-1.

Because Bi-FET bias current can increase by a factor of 1000 in going from 25°C to 125°C, it is necessary to change the input sensing resistors from 5 Ma to 100 Ka. Relay K8 is programmed for the high temperature measurement in order to cause the resistor value to change.

Although slew rate is not a static test, it was tested automatically with the parameters listed in Table 2-1. The test circuit for slew rate and transient response is shown in Figure 2-4. It is an easy matter to incorporate this circuit into the Figure 2-3 test circuit, however, care must be taken in routing the connections to the op amp inputs. Table 2-2 shows the test conditions and equations for slew rate and transient response. Because of limitations with the S-3260 measurement system it was not possible to measure noise and transient response automatically with the other op amp parameters. Bench set ups had to be used for these measurements.

Another parameter which had to be tested manually using the circuit in Figure 2-5 is settling time.

The op amp test adapter is shown in Figure 2-6.



NOTES:

- All resistors are ±0.1% tolerance and all capacitors are ±10%, tolerance unless otherwise specified.
- 2. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and change of state of relays (i.e. disable voltage supplies, current limit \pm $V_{\rm CC}$, etc).
- 3. Compensation capacitors should be added as required for test circuit stability. Two general methods for stability compensation exist. One method is with a capacitor for nulling amp feed back. The other method is with a capacitor in parallel with the 49.9 k Ω closed loop feedback resistor. Both methods should not be used simultaneously. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations, etc. Loop response and setting time shall be consistent with the test rate such that any value has settled for at least 5 loop time constants before the value is measured.
- Adequate settling time should be allowed such that each parameter has settled to within 5% of its final value.
- 5. All relays are shown in the normal de-energized state.
- 6. The nulling amplifier shall be a M38510/10101XXX. Saturation of the nulling amplifier is not allowed on tests where the E (pin 5) value is measured.
- 7. The load resistors 20500 and 11.1 k Ω yield effective load resistances of 2 k Ω and 10 k Ω respectively.
- Any oscillation greater than 300 mV in amplitude (peak-to-peak) shall be cause for device failure.

Figure 2-3. Test Circuit For Static Lests

	Units	A -				PA .					•				>	E13) PA
	Equation	v ₁₀ = E ₁	v _{IO} = E ₂	V _{IO} = R ₃	V10 = E4	-I _{IB} = 10,000 (E ₂ - E ₅)	$+I_{IB} = 200 (E_6 - E_7)$		+I _{IB} = 200 (E ₃ - E ₈)	$-I_{IB} = 200 (E_1 - E_9)$	$-I_{1B} = 10,000 (E_{10} - E_2)$	* * * * * * * * * * * * * * * * * * *	-118 - 200 (E12 - E11)	-I _{IB} = 200 (E ₁₃ - E ₃)	$^{-1}$ IB = 200 (E ₁₄ - B ₁)	I ₁₀ = 200 (2E ₃ - E ₈ - E ₁₃)
q	Units	Δ-			-										>	
Measured pin	Value	El	R ₂	33	B¢.	E _S	B ₆	E7	83	E9	E10	112	E12	E 13	B14	ata
Mea	No.	5													>	p gI ₁ -
Energized	Relays	None				к1, к8	None	ΚΙ	K1	кі	к2, кв	None	K2	K2	К2	Calculate value using $V_{{ m IO}},$ + IIB and - I $_{ m IB}$ data
es ers	4	-15 V	15 V	Λ 0	ο ν	15 V	10 V	10 V	Δ 0	-15 V	15 V	10 V	10 V	Λ 0	-15 V	sing V _I (
Applied Voltages Adapter pin numbers	3	Open														alue u
plied ter pi	2	- 5 V	-35 V	-20 V	- 5 V	-35 V	-25 V	-25 V	-20 V	- 5 V	-35 V	-25 V	-25 V	-20 V	- 5 V	late v
Ap		35 V	S V	20 V	5 V	5 V	Δ ς	5 A	20 V	35 V	λ ς	Δ 5	Λ S.	20 V	35 V	Calcu
	Notes	/7					/8					/8/				
Parameter	Symbol	v ₁₀				4I _{IB}					al-					In

Table 2-1. Test Table For Static Tests.

Symbol N		Adan	ter of	Adapter nin numbers		Franciored	2	Measurad nin			
	Notes	1	2	3	4	Relays	No.	Value	Units	Equation	Units
+PSRR		10 V	10 V -20 V	Open	^ 0	None	3	E15	>	+PSRR = 20 $\log \frac{10^4}{(E_3 - E_{15})}$	яр
-PSRR		20 V	20 V -10 V	Open	ν 0	None	i	913		-PSRR = 20 log 104 (E3 - E16)	
E S	3/	Calcu	late va	alue us	Calculate value using V $_{ m 10}$ data	data				CMR = 20 $\log \frac{3 \times 10^4}{(E_1 - E_2)}$	db
v _{IQ} AbJ (+)		20 V	20 V -20 V	Open 	> 0	К7	ç	E17	^	$V_{10} \text{ ADJ (+)} = E_3 - E_{17}$.⁄a
V _{IO} ADJ (~)		20 v -20 v	-20 v		^ 0	K6, K7		E.18		$V_{10} \text{ ADJ}(-) = E_3 - E_{18}$	
Ios (+)	/5	15 V -15 V	-15 V		-10 v	None	ع	1.	Æ	108(+) = 11	重
I _{OS} (-)		15 V -15 V	-15 V		10 v	None		12		105(-) = 12	
1cc		15 V	-15 v		Λ 0	None	2	1,3	щÀ	ا در = 1	Ą.
+V _{OP}		70 V	20 V -20 V	Open	-20 γ	K3	9-	(F ₀) 1	۷ -	+V(+ = (E ₀) ₁	-
-V _{OP}					20 v	кЗ		(E ₀) 2		-V _{OP} * (E ₀) ₂	
do∧+					-20 v	к',		(E ₀) 3		+V _{OF} = (E _O) ₃	>
-v _{OP}		->		>	20 V	7 2	->	(£ ₀) 4	-	(6.4) = 40A.	

Table 2-1. Test lable For Static Tests. (cont'd)

Parameter		Adapt	Applied Voltages Adapter pin numbers	oltage	S	Energized	, es	Measured pin	E.		
Symbol	Notes	1	2	2 3 4	7	Relays	No.	Value Units	Units	Equation	('nits
Avs (+)	41	20 V	-20 V	Open	20 V - 20 V Open - 15 V K4	7. 7.	5	E19	>-	Avs(+) = 15/(E3 - E19)	V/ex
Avs (-)					15 v			E20		$A_{VS}(-) = 15/(E_{20} - E_3)$	
Avs		5 V	5 V - 5 V		- 2 V			E21		$AVS = 4/(E_{22} - E_{21})$	Am/A
		5 γ	5 V - 5 V		2 V	>	>	E ₂₂	-		
NI (88)	19	20 V	20 V -20 V		Λ 0	KS	9	(£ ₀) 5	sw.rms	N1 (BB) = $(E_0)_5/1000$	UV rais
NI (PC)		20 V	20 v -20 v	>	۸ ٥	к1,к2,к5,к8		(£ ₀) ₆	шVрk	$NI(FC) = (E_0)_6/1000$	uV.pk
A V _{IO} / A T	17	Δ ^V 10/	' ΔT =	(v ₁₀	@ 125'	$\Delta V_{10}/\Delta T = (V_{10} @ 125^{\circ}C - V_{10} \stackrel{?}{3} 25^{\circ}C)/100^{\circ}C$	ot/ (o.	3° c			ον/ [,] C

NOTES:

- (For example: If $E_1 = 2$ V and $V_{10} = E_1$, then $V_{10} = 2$ mV.) The equations take into account both the closed loop gain of 1,000 and the scale factor multiplier so that the calculated value is in Table I units. The measured value units should, therefore, be used in the equation. 7
- Each device shall be tested over the common mode range as specified in Table 2-1. $V_{\rm cm}$ conditions are achieved by grounding the inputs and algebracially subtracting $V_{\rm cm}$ from each supply. (For example: If $V_{\rm cm}$ = -15 V, then + $V_{\rm Cc}$ = +20 V (-15) = +35 V and $V_{\rm Cc}$ = -20 V (-15) = +5 V. 7
- Common mode rejection is calculated using the offset voltage values measured at the common mode range end points. m

To minimize thermal drift the reference voltage for the gain measurement (E_3) shall be taken immediately prior to or after the reading corresponding to device gain $(E_1g,\,E_2g)$.

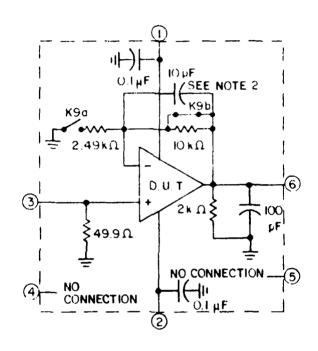
31

- 5/ The output shall be shorted to ground for 25 ms or less.
- 6/ Broadband noise NI(BB) shall be measured using an RNS voltmeter with a bandwidth of 10 Hz 5 kHz. "Popcorn" noise NI(PC) shall be measured for 15 seconds.

Ç

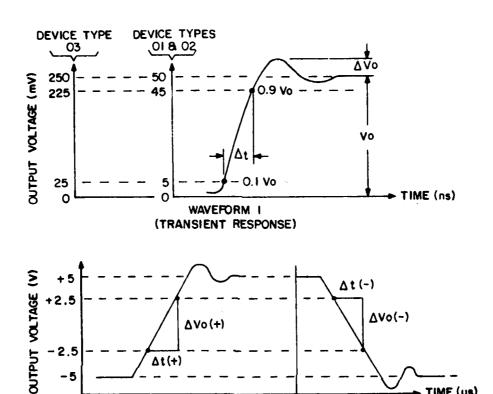
- 1/ Δν₁/ΔT drift between 125°C and 25°C is shown. Δ ν₁₀/ΔT drift between 55°C and 25° is calculated in a similar manner.
- For tests at 125°C, K8 is energized and the equation coefficient changes from 200 to 10,000. <u>س</u>

Table 2-1. Test Table For Static Tests. (cont'd.)



- 1. Resistors are +1.0% tolerance and capacitors are +10% tolerance.
- This capacitance includes the actual measured value with stray and wire capacitance.
 Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.
- 4. Pulse input and output characteristics are shown on the next page.

Figure 2-4. Test Circuit For Transient Response and Slew Rate.



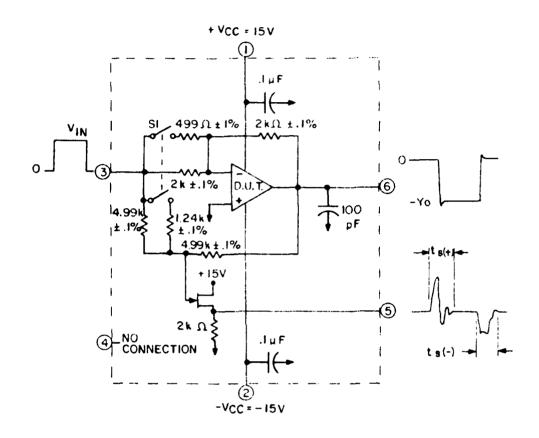
Parameter symbol	Device type	Input pulse signal 0 t _r ≤ 50 ns	Output pulse signal	Equation	
TR (t _r)	all	+50 mV	Waveform 1	$TR(t_r) = \Delta t$	
TR (e _s)	a11	+50 mV	Waveform 1	$^{TR}(o_s) = 100 (^{\Delta Vo}/Vo)$	
SR (+)	01,02	-5 V to +5 V step	Waveform 2	$SR(+) = \Delta Vo(+)/\Delta t(+)$	
	03	-1 V to +1 V step	Waveform 2		
SR (-)	01,02	+5 V to -5 V step -1 V to +1 V step	Waveform 3	$SR(-) = \Delta Vo(-)/\Delta t(-)$	

WAVEFORM 2 (POSITIVE SLEW RATE)

WAVEFORM 3

(NEGATIVE SLEW RATE)

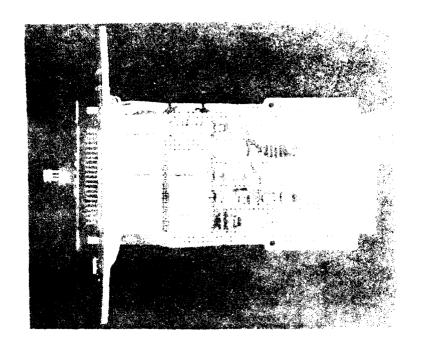
Table 2-2. Test Table For Transient Response and Slew Rate.



NOTES:

- Resistors are +1.00 and capacitors are +10° unless otherwise specified.
 Precaution shall be taken to prevent damage to the D.U.T. during insertion
- into socket and in applying power. 3. For device types 01 and 02, S1 is open, AV = -1 and V_{TR} = 10 V.
- 4. For device type 03, S1 is closed, AV = -5 and $V_{\rm IN}$ = 2 V.
- 5. Settling time t_s , measured on pin 5, is the interval during which the summing node is not nulled.

Figure 2-5. Test Circuit For Settling Time.



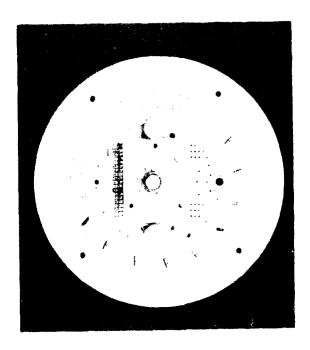


Figure 2-6. Bi-FET op amp test adapter.

2.4 Tabulation of lest Data

Shown below is a list of types and quantities of devices which were submitted by the I.C. manufacturers for characterization testing.

Device Type	Manufacturers *	Quantity
155	F, S	24
156	F, S, A	24
157	S, A, N	24
155A	N, P	9
156A	N, P, I	64
157A	P	20
355	T	9
	Total	204
		· · · · · · · · · · · · · · · · · · ·

F = Fairchild
S = Signetics
A = AMD
N = National
P = P.M.I.
I = Intersil
T = Texas Instruments

The devices were tested in two groups with the distinction being A's or non-A's. The non-A's were tested first. Improved limits on offset voltage, $\sum V_{10}/\sum T$ and slew rate are the essential differences between the two groups. Within each group the 155's, 156's and 157's have identical limits except for supply current, transient response and slew rate. Also, the 157 is an undercompensated device for use in wideband applications with a minimum closed loop gain of 5V/V.

The 355 devices were tested with the precision A parts, but the data was not statistically grouped with those devices.

A typical data sheet of an LF155 op amp in the first group of testing is shown in Table 2-3. All of the data is within the initial JC-41 committee recommended limits, unless an asterisk (*) is displayed adjacent to the measured value. For this group, the data at all three temperatures $(-55^{\circ}\text{C}, 25^{\circ}\text{C} \text{ and } 125^{\circ}\text{C})$ is shown on a single table.

On the second group of devices (LF155A series), it was decided to change the format so that the data of up to ten devices could be displayed on a single sheet. Table 2-4 shows this scheme for different devices at a single temperature. With this method it is easier to make device-to-device comparisons and to check for common peculiarities, etc.

A third form of data common to both groups of devices are histograms. Figure 2-7 shows a histogram of offset voltage V_{iO} at zero common mode voltage and 25°C for all of the devices in group 2. The raw data is too extensive for inclusion in this report, since each test group contains 114 histograms and over 30 individual data sheets. Besides showing the data elements v.s. frequency of occurence, the histograms also display the initial JC-41 parameter limits. Direct comparisons of the data to the proposed limits are useful in determining the relative test yields of the devices. The raw data was presented to industry representatives in two reports as follows:

- 1. Characterization Data for MIL-M-38510/114 Bi-FET Op Amps (Commercial Types LF155, LF156, and LF157) (21 November 1978).
- 2. Characterization Data for MIL-M-38510/114 Bi-FET Op Amps (Commercial Types LF155A, LF156A, and LF157A) (16 April 1979).

Within the static test parameters, the measurement and characterization of input bias current was the most difficult. Figures 2-8, 2-9 and 2-10 show how input bias current varies typically with common mode voltage, supply voltage and manufacturer. These figures were observed with a Tektronix Type 577 curve tracer. Figure 2-11 shows a similar bias current curve that was generated using the S-3260 with the op amp adapter. Increasing temperature can also cause an increase in input bias current as shown in Figures 2-12 and 2-13. The effect of common mode voltage on offset voltage is shown in figures 2-14 and 2-15. Figures 2-16 and 2-17 show typical small signal transient response waveforms of the LF155, LF156 and LF157. The effect of closed loop gain on the LF157 response is also shown.

Typical slew rate response for all device types is shown in figures 2-18 and 2-19. Settling time waveforms are shown in figure 2-20. Curve tracer displays of gain and noise are shown in figures 2-21 and 2-22.

Tables 2-5 to 2-10 are statistical data summaries of the LF155 and LF155A series devices at -55° C, 25° C and 125° C. These tables are useful in showing parameter yields to the initial specification limits.

Tables 2-11 and 2-12 show the distribution of data for most of the parameters in a cryptic histogram form.

Manual test methods were used to generate the dynamic data of the difference device types as shown in Tables 2-13, 2-14 and 2-15.

MANUFACTURER CODE: A) DEVIC	DEVICE TYPE!	165 , S/NI	A : DAT	DATE CODE!	1 29 NOU 78	22138131	31		1000
PARAMETER		-65 DEG C	#1 1-17F	10-118	DATA DATA	HI-LIM	LO-LIM	DATA	HI-LIM	
1110/-CM3 AT 3511511	9	-3.26	9		-1.33	•	-6.00	-13.34	3.	£
UIO(+CR) AT 50,-350	9.9	-2.62	8 . 9	-4.	E	3	9.9		21	₽i
UIOCOCH DAT ROU, -200	2.9	4) .	3 3		-1.16	3	9.9	-44.0H	28	3
D-UIO/D-T FROM 25 OC	-30.	22.5	9.0				-30.0	12.5	9.8	6 /90
US- 136 TA (#2-)011		•	***	-20.0	4.46	90.02	-20.eX	285	20.0X	ď
IIO(+CR) AT 50,-350	9		3.	2	-148.	. 00.	¥ 600	-3.04K	¥ 1	E
110(0CM) AT 200,-200	•	00.0	8.	-50.6	-16.5	• • •		1.345		E 8
IIO(+CR) AT 50,-250	9.00			P. 03'	4 0.451					
US- USE TO CHO-1911+	9.0	9.00	96.0	-100.	11.2	199.	-18.9K	7.79K	50.0K	g,
+118(+CH) AT 5U, -35U	0.0	0.00	8.08		1.07K	2.00X	-10.ex	18.5	3 : 3 :	4 6
+118(0CH) AT 280,-280	99.9	9 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6	8.6		7 U	. 66	- 16. G	11.61		3
+IIB(+CH) W1 50,-250	99.	9			9					:
4	6	98.9	9.00	-100.	6.71	3.	-10.0K	7.51K	50.0K	£
6	6	00.0	0.00	-100.	1.215	₽. ₩	-10.9X	21.4K	20.0¥	Œ į
4	•	3	9.00	-100.	4.99		-10.8K	13.18	20°	Œ
-118(+CM) AT 50,-250	0.00	8.0	2	-100.	163.	386.	-10.0K	13.8K	5 0.0 X	£
	0	901	9	6. C.	110	8.6	85.0	115.	3	8
-PSKR AT 180, -CEO	00 00 50 00 60 00	112.	90.0	85.6	108	96.	85.0	114.	3	4
		,		9	7 30	8	×	5.79	9	9
CHE AT COOCOO	82.6	A 17. W	9	9		3) })
U-45.14+) AT 280, -280	8.96	13.0	30.0	8.60	13.0	2 0 .0	8.00	13.1	9.0	2
U-ADJ(-) AT 280,-280	-50.0	-14.3	-8.60	-20.0	-14.3	-8.86	-20.6	-14.6	9 . 20 -	2
10672 07 1611 21611	6	£ 65-	6	-60.0	-24.6	8.	-60.0	-15.0	8.6	ş
105(-) AT 15U15U	00.0	36.00	9 . 9 9	2	. SS	60.09	0.00	16.7	66.6	£
	6	,	•	•	9 6	8	9	50.5	4.00	٤
100 AT 150, 150	9 6	1 U	9.0	9	. T.	3	9	3.31	2.8	ş
וכר או כפסי בפס		;	•	•					į	;
Œ	16.0	18.2	20.0	16.0	18.5	20.0	16.0	œ (9. 9. 9. 9.	>
4	-88-	m.e.	16.0		900	- a - a - a - a - a - a - a - a - a - a	- C	0.00	50.0	• >
-UOP AT RI-SK	. 600 i	-17.6	-15.0	9.00	-17.00	-15.0	-50.0	-17.5	-15.0	>
20 10 10 10 10 10 10 10 10 10 10 10 10 10		i du		9	1.000	88	5 2.	. 596	:	₹/A
AUC - 1 AT B1 - 1 AK		7.00 T	96.6	9	100.4		25.	3.334	:) E
AUS(+) AT RL-2K	25.0	1.50K	9.0	20.0	1.50K	0.0	25.4	969	3	2
AUS(-) AT RL-BK		1.50X	9.00	50.0	. 600	•	25. 0	21g.	3 1	
AUS AT 50,-50, RL-10K		-		9.6	¥.	9.0		7		
AUS AT 50,-50, RL-2K		•				3			;	:
SR(+) AT 280,-280	8 :	11.8		8.0	33	33	3 1	7.8	31	22.5
SR(-) AT 280,-280	2.	59.4	9.0	, i	•		3		3	;
HOTES:1.ZERO (8) IN LI	INITS COL	JAN HEANS	INITS COLUMN MEANS NO LIMIT. IT CAN BE INTERPRETED AS	AN BE INTE	RPRETED AS	A DASH (-).				

Table 2-3 Typical LF155 Op Amp Data Sheet

BI-FET OPERATIONAL AMPLIFIERS	IFIERS -	166A J	TEMPER	TEMPERATURE: +26	S DEG C	DEG C , 04 MPR 78 Vendor Code A	19 14146116 P A	9.					
	-C3-	:	=	2	=	2	.	ă	3	6	3	HI-LIM UNIT	5
VIO(-CR) AT 350,-50 VIO(-CR) AT 50,-360 VIO(-CR) AT 50,-360 VIO(-CR) AT 50,-60 B-VIO/-T FROM 86 OC	*****	40.400			1070 0000 0000 0000 0000		# # # # # # # # # # # # # # # # # # #		#2548 #4544	#### ####	2.04.0 2.04.0 2.04.0 2.04.0 3.	*****	55553 6
350, -50 260, -350 260, -350 360, -350		-166. -166. -158	121. 121. 13.36.3	4822 4832 • 6446 *	-91.2 -6.73 -16.73	82.8 9.63 -23.8 -235.8	26.8 -7.7 -17.1	55.8 5.92 4.75	20.00 20.00 20.00 20.00 40 40.00 40 40.00 40 40 40.00 40 40 40 40 40 40 40 40		959.R -101. -8.91	2400	2222
350, -50 50, -350 280, -280 60, -250		6.56 1.64K 66.4 128.	4.4.6 4.4.6 46.1 91.7	33.3 856. 72.6 103.	26.0 1.04K 41.5 74.1	54.6 1.17K 85.9 118.	16.8 1.37K 43.5 86.9	12.3 1.27K 39.8 85.0	46.1 754. 83.0	8.81 1.65K 37.0	16.8 1.52K 38.5 82.7	30.50 80 80.50 80 80 80 80 80 80 80 80 80 80 80 80 80	::::
350, -50 50, -350 260, -260 50, -250		-6.14 1.80K 65.1 135.	18.8 45.3 85.1	87.8 53.2 84.8	15.7 1.13K 90.3 0.3	31.8 1.23K 76.2 119.	6.58 1.47K 51.2 104.	1.76 1.33K 33.9	23.1 745. 64.5 91.9	6.62 1.86K 61.3 129.	15.2 1.62K 47.4 95.7	36.55	1111
AT 180, -280 AT 280, -180	85.0 85.0	117.	120. 122.	111.	169.	1 88 . 1 <i>0</i> 6.	132. 1 0 7.	169. 186.	114.	115. 200.	110.		44
	85.0	29.7	166.	97.3	111.	102.	88.1	94.1	92.3	2.96	95.4	9.99	7
105(+) AT 15U,-15U 105(-) AT 15U,-15U	-50.0 0.00	-19.6 18.7	19.5	-20.9	-21.5 21.5	-20.9 18.7	-17.4	-20.4 20.5	-21.3 20 .7	-19.9	-20.5	50.00	2
		3.83 3.66	3.16	3.25 3.64	3.23 3.61	2.3 9	3.32	3.74	3.66	2.75 3.00	3.81	** **	£ £
	100.00	4.00.00	45.44	21 1 1 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	4 10 44 4 10 44	4.00.00 4.00.00 4.00.00	21.1.1 80.80.1.	2.5.5	12.00.0	# 55 4 # 2 4	-18.4 -17.4	26.6 26.6 15.6	2222
AT RI-10K AT RI-10K AT RI-10K AT RI-10K T SU-15U, RI-10K T SU,-5U, RI-10K		88.00 80 80.00 80.00 80.00 80.00 80 80 80 80 80 80 80 80 80 80 80 80 8	XXX	4 66 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	**************************************		1.50K 1.00.K 1.00.K 420. 1.14K 1.14K		7.00 7.00 8.00 8.00 8.00 9.00 9.00 9.00 9.00 9		968. 100.8 1.00.8 5.00.0 5.00.0 5.00.0	*****	>>>>>> 555555
200,-200	## ##	7.14	6.58 14.5	21.3	9.01 23.8	 	7.87	7.07	10.1	13.9	7.94		55
200, -200 200, -200	# * * * * * * * * * * * * * * * * * * *	13.0		-14:8	12.5	-14.3	-14.3	-14.2	13.0 -14.3	-14.3	226.Nt	•:	22
IN LIR	NOTERILIERO (8) IN LIMITS COLU	HN MEANS	NO LIMIT.	IT CAN BE	INTERPRE	TED AS A	DASH (-).						

Table 2-4 Typical LF155A Op Amp Data Sheet

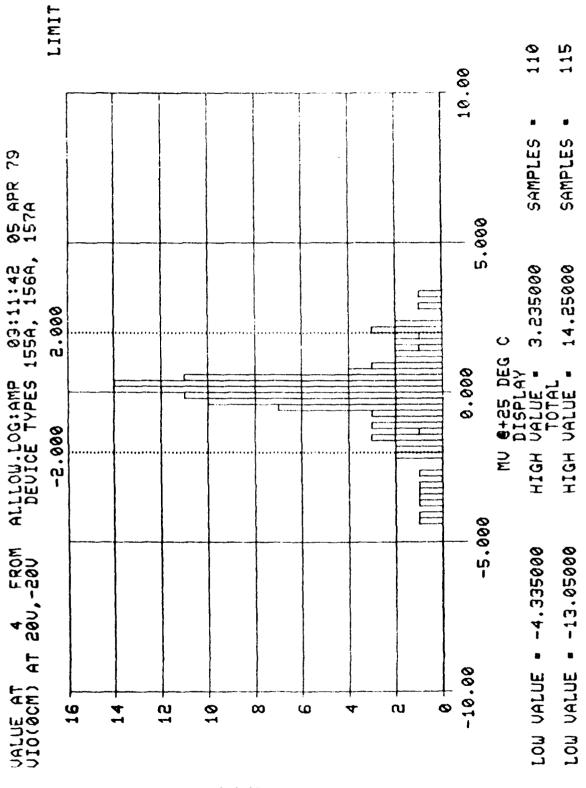
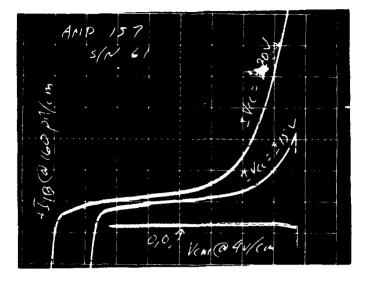


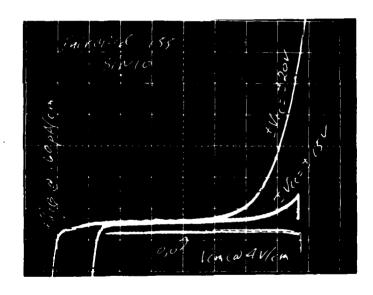
Figure 2-7 155A Series $V_{\mbox{io}}$ Histogram



+I_{iB} @ 160 pA/cm



 $V_{cm} \subset 4V/cm$

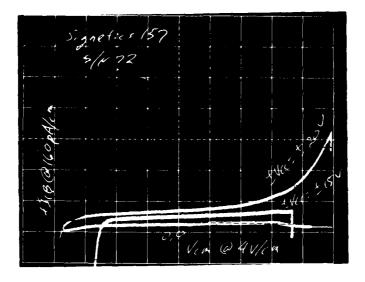


V_{cm} @ 4V/cm

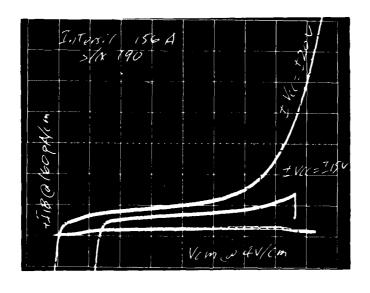
Figure 2-8 Bi-FET Input Bias Current vs. Common Mode Voltage



+I_{iB} @ 160 pA/cm



Vcm @ 4V/cm

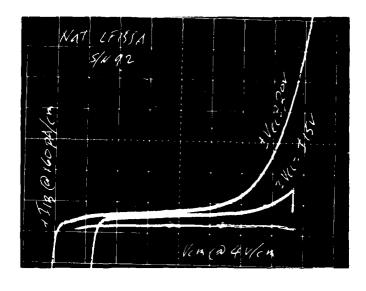


Vcm @ 4V/cm

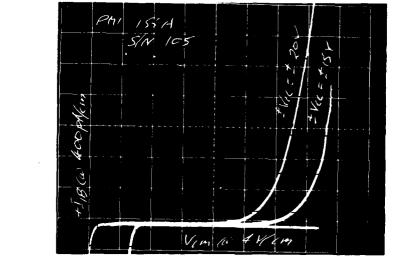
Figure 2-9 Bi-FET Input Bias Current vs. Common Mode Voltage



 $+I_{\,\mathrm{i}\,\mathrm{B}}$ @ 400 pA/cm



 v_{cm} @ $4v/c_m$



 v_{cm} @ 4v/cm

Figure 2-10 Bi-FET Input Bias Current vs. Common Mode Voltage

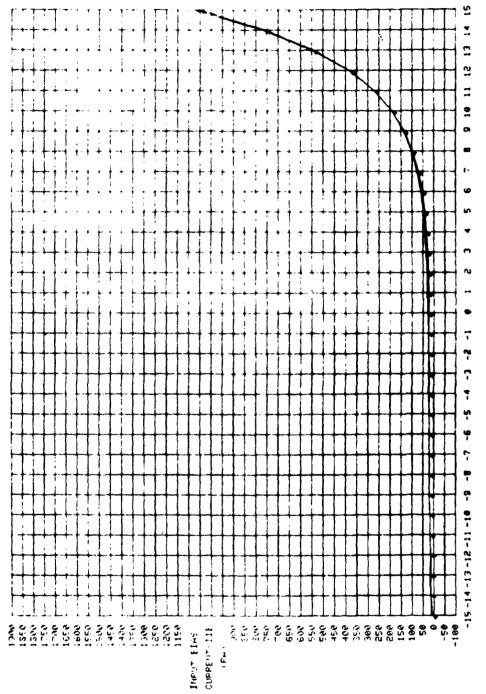
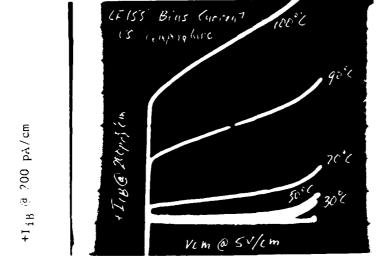


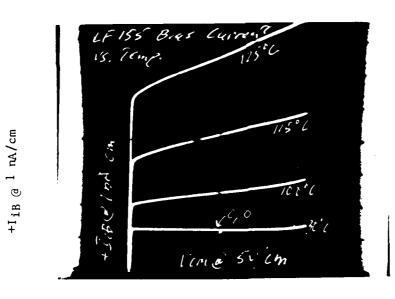
Figure 2-11 Bi-FET Input Bias Current vs. Common Mode Voltage



 $+I_{iB} = 1120 \text{ pA}$ @ 100°C, $V_{cm} = 0V$

V_{cm} @ 5V/cm

LF155 Bias Current from 30°C to 80°C



 $+I_{iB} = 5.2 \text{ nA}$ @ 125°C, $V_{cm} = 0V$

 $v_{cm} \approx 5v/cm$

LF155 Bias Current from 30°C to 125°C

Figure 2-12 Bi-FET Input Bias Current vs. Temperature

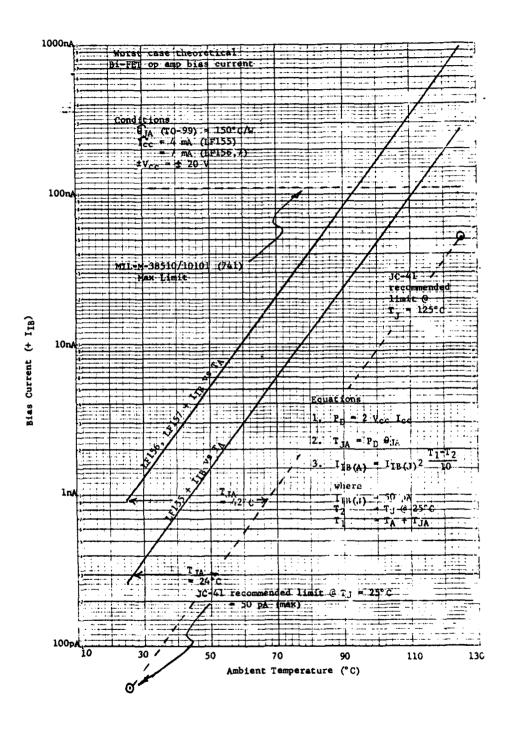


Figure 2-13. Worst Case Input Bias Current vs. Ambient Temperature.

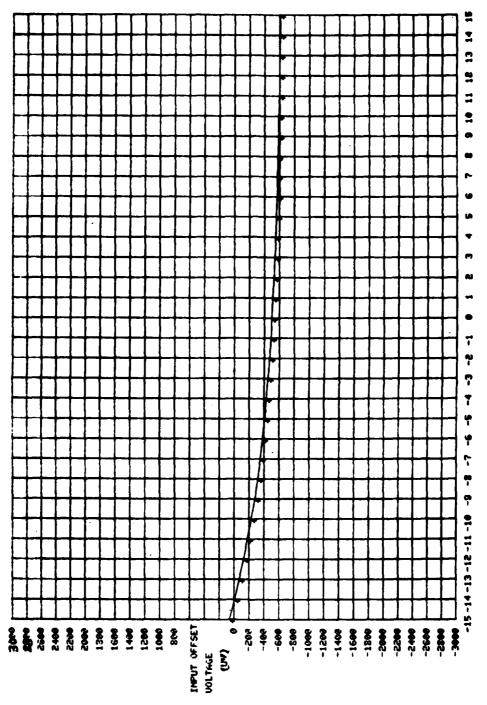


Figure 2-14. Offset Voltage vs Common Mode Voltage. II-26

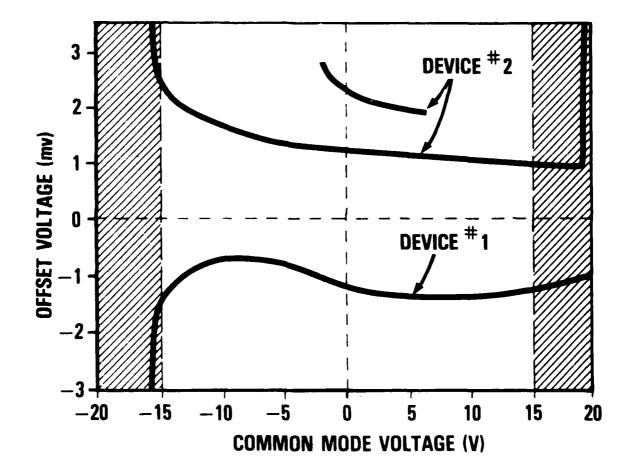
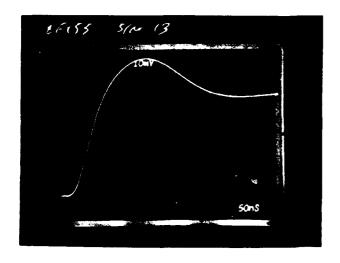
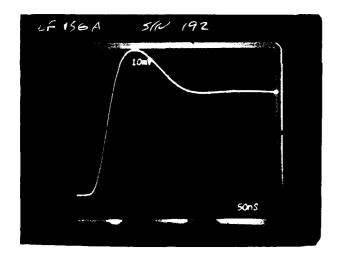


Figure 2-15. Offset Voltage vs Common Mode Voltage.

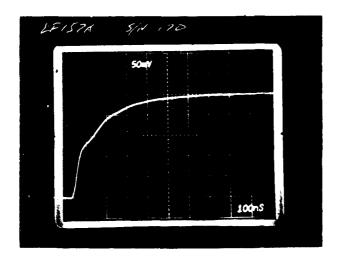


Typical LF**1**55 TR (tr) = 60 ns TR (OS) = 34° GBW = 5.8 MHz A_V = 1 V/V TR (tr) x GBW = .348



Typical LF156A TR (tr) = 40 ns TR (OS) = 38% GBW = 7 MHz A_V = 1 V/V TR (tr) x GBW = .350

Fig. 2-16. LF155 & LF156 Transient Response.



TR (tr) = 300 ns TR (OS) = 07 GBW = 1.1 MHz A_V = 5 V/V TR (tr) × GBW = .330

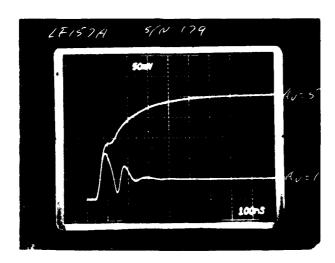
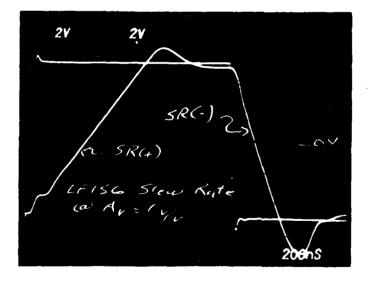


Fig. 2-17. LF157 Transient Response.

SR(+) = 4.7 V/us SR(-) = 10 V/us (SR = ... V/... T = 0 V from -2.5 Vto + 2.5 V)

500 ns/cm

LF155 slew rates % AV = 1 V/V



SR(+) = 14.3 V/us

SR(-) = 33.3 V/us

(SR = \triangle V/ \triangle T @

V from -2.5 V to

+ 2.5 V)

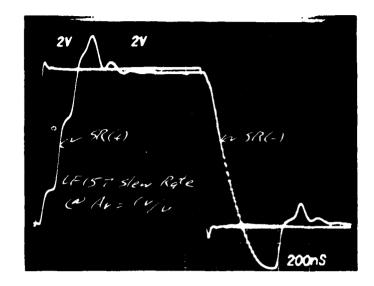
500 ns/cm

LF156 slew rates @AV = 1V/V

Figure 2-18. LF155 and LF156 S lew Rates. II-30

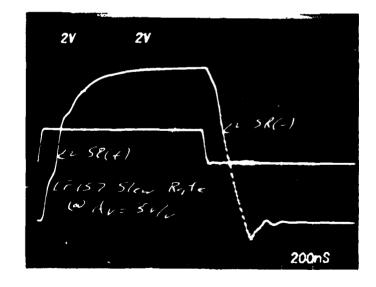
2 V/cm

2 V/cm



SR(+) = 40 V/us SR(-) = 50 V/us $(SR = \triangle \text{V/} \triangle \text{ T})$ V from -2.5 Vto + 2.5 V)

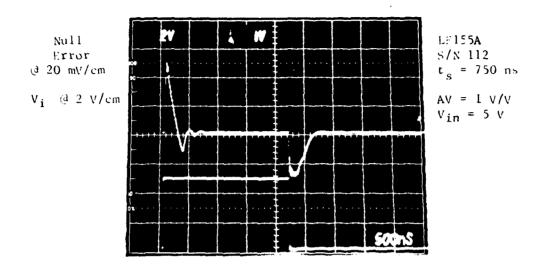
LF157 slew rates (d AV = 1 V/V



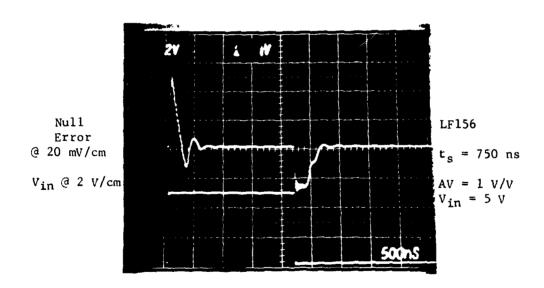
SR(+) = 33 V/us SR(-) = 50 V/us $(SR = \triangle \text{ V/} \triangle \text{ T } @$ V from -2.5 Vto + 2.5 V)

LF157 slew rates @AV = 5 V/V

Figure 2-19. LF157 Slew Rate vs Gain. II-31



Time @ 500 ns/cm



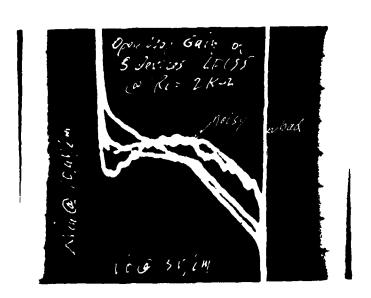
Time @ 500 ns/cm

Figure 2-20. LF155 Series Bi-FET Settling Time.

 V_{in} @ 10 mV/cm

 V_o @ 5 V/cm

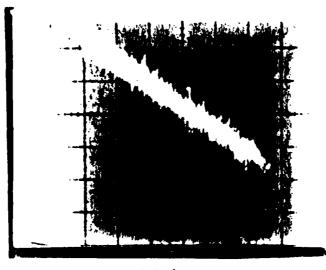
LF155 Open loop voltage gain $A_{\rm VS}$ (+) @ $R_{\rm L}$ = 50 K $_{\rm A}$



 v_0 @ 5 V/cm

LF155 Open loop voltage gain $A_{\rm VS}$ (*) @ R $_{\rm L}$ = 2 K $_{\rm LL}$

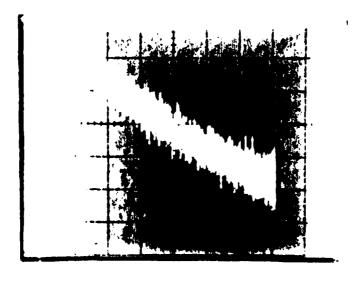
Figure 2-21. Open Loop Voltage Gain vs Load. II-33



LF155 S/N 19 $R_S = 50 \, \Omega$ NI (BB) = 10 uV_{pp} = 1.67 uV_{rms}

Vo @ 5V/cm

* Note: Random noise has a Gaussian amplitude distribution such that the ratio of (peak to peak) over (rms) is 6 and will not be exceeded 99.37% of the time.



LF155 S/N 19 $R_S = 50 \text{ K}_{\Lambda}$ NI (PC) = 0 uV_{pp} = 0 uV_{rms}

Vo @ 5 V/cm

Figure 2-22. LF155 Series Bi-FET Noise Voltage.

diatighted mines		- 111	5 B	÷ ′.	Space	L	27 15	2	15:20:19	61						
DA4246 15 2	11.38 v	177.00 VAL ::#	şıx '	15.P.	4715 412F	3 1 5 4 5 3 1 5 4 A	\$ 17. \$ \$16.44	2 F 4 E1	11,17	L0.		* FAIL FIGH 2,	11217	# 1 6 4 # F. J	<u>:</u> آ	
								7		;	•	•	:	:	:	;
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0000	1.47	274.5	70.0	ž	45.2	1.0.1	(, 0	60.5-	c • c -	44.	e 0 ° 0	5,00	٠,٠	2.12	>
2101412 BF 451145	4	2	٠١٠٧	7.	٠,	93.5	7.0	٠,٠	65.34	0.01-	۲۰۰۶	-,-	60.5	٠,٠	1.97	>
	5 7 . 7 .		. 025	₹ C •	ř	٠,٠	100	e .	00.5	0.0		ć .	5	0		> ¥
-	-4.17	4.10	544.	٥,٠	}	4.7		Ę.	٠, ٠,٠	-10.5		ز ا	ر. د	c .		> : > :
110(-C4) AT 354-5.	٠٠.٠٠		ī. C.	- =	4	6.10	٠,٠	- ·	0.00				c c (, :	0.0	· ·	4 .
110(+C4) AT 50.+55	-6.44		P. 17.0	1 4.4.	-	٠.٠	ć.,	-(-400-				*00°	3.64	4
1 (0 (0 (v) at 2012	-41.7	41.2	41.1-	0.0	7	0.7	٠,٠	3	0.04	140.	a		٠	6		4
۳.	٠.٠١-		5.06-	=	?	4.7	۲.			0 0 0	5	7	c .	6.6	2 6	A .
1.4	5.15.	1.1.	2.0	- -	Ç .	α /	- c			001-		4.6	· ·		ζ.	•
+118(+C") A1 5v,-14.		7.03K	047.	717	? :		100			006	7		C			4 6
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		• • • •	7 7 7		7	6.16	2,		00	001	65.4	7	. v L %	600	5, A.A.	44
1							95.2	٠,٠	5.5	0.0	4.34	, c	¥00.	1.10	25.5	#6
2001 200 He 0000	· c		117.	γ.		60.00	4.5		A5. 1	60.0	3.71	0.0	¥00.	140.	221.	ra G
2001-200 F4 241	0 + 2	0.5	102	0,0	٠,	9,,0	101	1.31	6	40.0	١. ١٠	00.0	7.00 C	. 691	194.	10
\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	c • • •	1 3 1	13.1	2.04	ç	45.2	100	c	, J	0.00	2.44×	00.0	900	٠.٠	91.7×	>
V-401(=) 41 20V-2	₩.	7.7I-	-14.	2.04.	4,	45.2	1001		-700	v * u 2 =	91.10	0,00	60.4	c c	3.078	>
179(+) 41 154-157	0	- I W ! -	-22.1	- a	ç	21.5	~ «	ر, ،	. · · · · · ·	0.04-	15.2		¥ 0 0 0	c •	556	4 5
10S(-) AT 15415V	05.0	7ª 4 C	22.7	3.13	3	7,40	7.40	ر.	¥00.	0.00	\$27.	00.	٠,	c :	5,12	4 1
ICC AT 150,-150	7.24	4.75	4.17	۲.۲	?	, a	7° 40		:	\ .	:			ر د د	3	4
TO AT PLETON	13.4	x -	1 A.	£ 5° 6%	ž	- 00	• o o •	0.0	e	9-0	2	c .	000	c .	4	> :
-VAP AT PLEIOK	-14.7	-17.7	-1 A.S	152	Ç.	T	- -		000			-		- c		.
	14.1	£.	٠.٨	7. 7.	Ç	٠ د د د د							· ·	200		• :
LUND AT HLEPK	A	-17.3	417.4	7	÷ ;		* ·									, ,
AVS(+) AT PLETOR	375	4.	×	× ;			, ,							0.0	4	> >
405(-) 41 PL=10K	×05.	40°C	***		<u> </u>		. 40					,	1001	¥ 0	10	>>
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2004 (a) 14 (b) 15 (c)	• 0		27.	90		20.00	7.94	0.00		00.0	1.32	7	13.0x	, 00°	1.07	\ \\\
20 1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2			20.0	4	÷	74.2	74.7	0.10	10.1	00.0	1.50	- ¥-	-	1.004	33.1	^1/ ^
TOTAL SOCIETY OF		• •	20			67.7	0	0.0	60.0	2.00	0 ° 2	20.00	1 25.0	25.0	9.75	511/1
VOVE - VOVE - + 1 A V V V V V V V V V V V V V V V V V V		- 5	. 4	40.0	ş	50.0	53.2	0.00	2.00	2.00	3.13		25°4	25.0	1.40	SH/A
				•												
NOTES: 1/ * Exclude	Ŋ	population		outside	le of	No	rej	4/ The		% fail for Icc		and S	and SK on this		table a	are
and high	re							not		d since	ce all		device types	es are	е сошр	compared
	•	,					,	to	type	10	limits.					
21 9 621	1 1	٧ ، وورا	5.7	o circled	, נים				:							
SA 1181 % /2					2			5/ The	There is	0	ts no maximum fail limit for pain	fail	limit	for		pue
3			106:21	•			•					1		- 1) :
3/ F1gur		eric	meric delinitions	r rous				'n	PI MUIO							

3/ Figure of merit definitions:

LO - FM = Z - low limit

HI - FM = High limit - X

Table 2-5. 25°C Statistical Summary or LF155 Series Devices.

4/ The % fail for Icc and SR on this table are not valid since all device types are compared to type 01 limits. 1/ * Excludes population outside of low rej and high rej NOTES:

2/ % fail values ≥ 5% are circled ◯

3/ Figure of merit definitions:

5/ There is no maximum fail limit for gain and slew rate.

LO - FM = X - low limit

O - FM = High limit - X

lable 2-e. -150 Statistical Samony For 10155 Series Devices.

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		00.0	0 0 7	~ ~	ž	£ 07	4		-7.99	-10.0	57.	4.	7.00	10.0	2.72	3
-	4.17	7.7	,	2.7	7	٠٠,٠	7° 40				, 44	<u>-</u>	7.00	10.0	۲. ۳	>
	-4.72	A.1.	¥6.0 ×	۲.۲	3	45.2	₹.			c - c : -	3.44	1.1	7.00	10.0	2.75	>
	21.05.	17.04	2.3.tx	¥ 2.5.	<u>.</u>	·.	٥.	<u>-</u> (-40.0x	٧٠,	7 ·	2	30°08	٠ ، د ،	4
4	14.61	24.34	140	A	£	1 H T	ĵ.	<u>ئ</u>		¥0.0%	2.60	٠,٠	ž.	C .	N. 4. 5	4
	-17.4K	\$0.4K	1.0°	7.14	7	٠٠ • ٢	٠.	- ·		Y 0 0 7 1	٨.	a (¥	40.0K		4
11n(+C+) AT 5v>5v	-31.2×	*h.1×	176.	7.184	Ē	٠. د	5	7		¥0.08-	A	= (1 	¥ .	¥0.00	£ ;	4
-	2.014	74. 4K	30° EK	۲.۰۲	ç	· ê	a .	c .		¥0.0	7,		, o	Y		4
+118(+C4) AT 50,-35V		77.08	7	¥ .	7 I	75.4	7. H			Y		Ž	٠ د د د	e c	~ .	4
۳		74.4K	22°4×	~~	ζ.	C 1	· ·	0.0		30°01-	 	7				
7	* 1 0 ¥	77.5K	2	Ž.	£ ;	· ·	· •			4 6		Ĵ			2	
- 1	ž .	¥ .	×	,	è	, a					77	Ý			•	4
₹ :				•	- v	. ~	200	6.0		0.0		Y.		40.04	-	. 0
2001 19 14 19 19 19 19 19 19 19 19 19 19 19 19 19		7.8.5.					95.5			10.0K	1.57	e.E.) i	¥ C * C *	1. 35	4
**	4	- 4	101	0,	7	5.15	94.			50.0	3.47		,000		- 6	ď.
VOT- 100 PL 200-	7		10.	· =	٤,		1110.	3.2		50.0	65.0		¥00.	_	150.	<u>م</u>
707- 707 17 170	2.50	124.	4.16		?	6.16	100	(a)		6.05	¥0.		¥00°		-	1
V-401(+) AT 20V26V	1.5.0	13.1	13.1	2.A14	3	٥٠,	98.		÷ ,	ر د و د	A C R .				4	> :
V-AD3(-) AT 20V,-20V	-1-1-3	•	٠	, ·	<u>ئ</u>	45.7	T. C.									i
10S(+) AT 15v,-15v	- ;	4.6	-13.7	7.	<u>}</u> ?	,	7 0				2000				9 4	. >
105(-) AT 150,-150	, , ,	2			u a							15.5			0	4
TCC AT 150,-150	7	0	, ,		2		. n	00.0		4	3.0.5	5	000	ر د د	*	· >
**************************************			- a	245	3	4.40	98.	0.0		0.02-	5 B S		c . 4 -	-14.0	10.2	>
	17.4		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	> 1 ~		38.0	100			15.0	10.4		• U U <	٠,٠٧	, , ,	>
	-17.A		-17.2	277.		5.5	9 A G	00.0	-500	-20.0	551.		0°51•	-15.0	7.	>
AVS(+) AT ML=10K	65.5		11.11	1.114		30.5	٠,٠	9.40	٠ د.			c .	٠. د د	10.C	ر مر ع	?
4/S(-) AT 41 =10K	32.1	10.0K	7.05k	2.154		77.4	c	c .	5.0	c (200	C .	,		, ;	>
AVS(+) AT PL=24	7 . K	A. 33F	1.05×	1.74		-		=			, ,					A
AVS(-) 4T PL=2*	1.07	1.47K	H C	317.	è :		,		(:		7		, y			> 3
AVS 47 5V, +5V, 4 = 10K	\$ 9.5				r u						,			¥ 6 6	117	
AVS AT 54.050.01=28	e :	• • • • • • • • • • • • • • • • • • •	• [75 -	,			
54(+) AT 20V,-20V	7.0	,			;		7 6									
34(-) AT 204,-204		· .	÷.		,		,	•	:	•	;		•	:	•	•
NOTES: 1/ * Exclude	ludes	population	trion	outside	de of	low	rei	4/ The		% fail for	r Icc	and SR on this	R on (table	are
				 					t val:	valid since	ce all	device	se ty			compared
		•						to	type	0	limits.					
2/ 7 fail va	1 valu	lues //	5% are		circled											
							•	5/ Th	pre 1	There is no maximum fail limit for eain	2 x 1 m 1 m	fail] fm f	t for	0210	מים
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Table 2-7, 125°C Statistical Summary For LF155 Series Devices.

 $LC - FM = \overline{X} - lou limit$ $HI - FM = High limit - \overline{X}$

view vice X View view vice X View view view vice View view vice X View view view vice X View view view view view view view view v	1				;		;										
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77.7 190. 119. 4.59 100 44.1 1947 470.4 45.0 40.0 15.4 0.0 2.0 10.0 2.0 10.0 10.0 2.0 10.0 10.	V-118(+C4) 41 5V25V		406	124.	53.8	Ξ	40.4	A . DC	0.10	-100	100	3,75	(c)	\$00	, u +	11.0	4
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1150201 -11.1 -11.4 -11.1 -11.1 11.1 04.7 04.0 -20.0 -20.0 15.4 0.15 0.0 0.0 1 11.1 11.1 11.1 04.7 04.0 0.0 0.0 1 11.2 0.0 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1	1-40J(+) 4T 20V20V	7.466	13.1	12.0	۲.	-1-	5 HO	98.3	1.7"	6.0	0.0	4.11	c .		ν. ν.	<u>:</u>	>
	1-401(-) AT 200,-200	-1.1.	-1.84	-14.1	-	Ξ	95.7	45.7		->00	0.05-	154.	4.15	01.1	٠,٠		ś
115.4.15	104(+) 41 154,-154	-24.	00.0	-21.7	5. 35	-11	٠,٠	97.4	00.0		-60.0	۶,۷	00.6	1.004	0.13	: ::	4
\$\langle{v}_{1} \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V21-141 14 (-)801	K . C .	74.0	7.5	٠ د د	-15	1. Te	100	٠ د	-1.30K	0.0		د	د.	٠,٠	•	3
## 113.1 13.5 13.4 13.5 13.1 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5 13.4 13.5	ICC AT 15v,-15v	2.5	٥. ،٥	4.1	٠,٧	~	~ ·		•		2.0	:	9	ر د ۱	٤.		4
##==nx	VOP AT RESTOR	· -	٠ <u>٠</u>	3 (7.	= :	÷ ;	24.5			C	- 1			,		•
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# #===================================		17.7			5.5	= :	5	-		· ·			5	2			>
	-VAP AT RL=24	-13.0		-17.5		- :	· ·		c :		0.0	2	2	c	5		>
	BVS(+) BT R[=10K	5.6.5	***							-		, .				,	•
	10 K 1 K 1 K 1 K 1 K 1 K 1 K 1 K 1 K 1 K	200	¥ 0 0 0 0					E 0		- (4)			•	
1/ * Excludes population outside of low rej 4/ The % fail for I _C and SR on this tab and high rej and values \$\frac{2}{2}\frac{7}{2}\frac{7}{2}\frac{1}{2	AVE(+) AT BUEN	134	10.08				6 f									· .	> :
2/ 7, fail values \$\infty\$ 53, are circled \$\infty\$ 7, fail values \$\infty\$ 53, are circled \$\infty\$ 7, fail values of merit definitions: \$\infty\$ 24,7 \\ 24			¥0.5°	×	. :			. :									>
1/* Excludes population outside of low rej 4/ The % fail for I _{CC} and SR on this tab and high rej 5% are circled 5/7 fail values 5/8 are circled 5/7 figure of merit definitions:	AVS AT 50, -50, 41 = 104		1		•											. ;	?
2/ 7 fail values = 5% are circled (2) There is no maximum fail limit for gas 3/ 10 for	TAT 34.45. 14 SAU		• • • • • • • • • • • • • • • • • • •	· (,	- 2		,								•	> .
<pre>1/ * Excludes population outside of low rej 4/ The % fail for I_{CC} and SR on this tab and high rej and high rej 2/ 7 fail values ≥ 5% are circled</pre>	84(+) AT 20V20V	50.0		, \	-	,						()	^\	()	(-
<pre>1/ * Excludes population outside of low rej 4/ The % fail for I_{CC} and SR on this tab and high rej not valid since all device types are to type 01 limits. 2/ 7 fail values > 5% are circled</pre>	54(-) AT 204,-204	- -	70.0	7 ·	3.52	~	- 65	55.7	ē.	٠,٠	۲.	3.55	75.0	٠,٠	٠. ٧		S=/>
and high rej and high rej to type 01 limits. 2/ 7 fail values \geq 5% are circled $>$ 5/ There is no maximum fail limit for gas 3/ Figure of merit definitions:		v.	popula		utsid					/ fa	41 for	-	and S	00	hist	ahle ,	4
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5% are circled	a pure		_						100	rvall	° _	e all					ared
1t definitions: 5/ There is no maximum fail limit for slew rate.	2/ 7 fat	lvalue	٨١			led)			•					
merit definitions:	i	•								re is	no ma	x f mon	fail	limit		eain :	pu
	3/ Figure		prit d	pfintt	ione			''		100	4		! !				} !
	1091 /)						;		,						

LO - FM = \overline{X} - low limit

HI - FM = High limit - \overline{X}

Table 2-8. 25°C Statistical Summary For LF155A Series Devices.

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VINCECM) AT 150,-5.	-7. 19		1.24	2.17	00:-	47.4	a		12.50	٠.٠	57A.	66.5	2.50	10.0		>
VIO(+C4) AT 54,-45.	* 7 · 4 ·		** < \ X =	٠. ٢	- 1	17.4	18.1		05.4	-10.	700	A: 25	٠	0.01		>
VID(000) AT 2048-2	* 4.0-	2 R P	1.21	<u>۲۰۱۰</u>	110	7.44	44.7	C.	(.5.6.	0,01-	3.5.5	6. Y	•	0.01		>
VID(OC#) AT SV 5.	4	42.0		7.13	=	7.40	α σ	P.E	05°C=	· • • •	1.03	6	7.50	10.0		3
V-ADJ(+) AT 20V,-2".	1.19	1.4.	0.61	1.09	===	¥ . 10	94.3	·:	c c .	0.00	15.7	ج د	v	20.0		>
V-ANJ(-) AT 244,-7 .	-12.4	-1.70	-14.1	-1.	Ξ	1.50	44.1	۵. ع	->4.	0.06-	154.	4.15	00.00	00.		3
198(+) 47 154,-157	-37.0	c • •	٠, ۲۰	4.95	115	24.5	97.4	· .	0.05	0.04-	3.14	0.0	1.003	000		٧.
105(-) AT 15v,-15v	,,	11.1	71.7		115	≥ . H C	1 0 u	,	-1. JOK	00.0	211.	00.0	0.05	, ,		7
ICC AT 150,-150	ō	7.51	9.3	02.	ž	7.84	77.4	:	:	7.00	:	A	4.30	A O		;
+VOP AT PLEIOK	c	~ * -	18.	34.74	=	a	05.1	4. 19	15.0	14.0	57.1	0.0	200	, 04		>
AVOP AT RESION	α	4.41-	-18.7	406.4	- 1	0.7.0	97.4		->11	0.02-	101	1.70	-15.0	(4 1 4		. >
+VOP AT BL=2K	17.5	C # 1	17.4	110.1	=	1.50	٥٠,٥	4.19	15.0	15.0	75.0	00.0	200	50.05		. >
-VAP AT CLEPK	-17.7	-14.4	-17.4	1.61	114	97.4	, a.		.016-	0.06-	: 17 6	470.4	6.15	6.51		· >
474(+) AT DIE10*	د	10.0K		×14.	103	45.2	٠. ٩٨	60	75.0	c c	417.	0.0	¥.	0.01		>> >
AVS(-) AT HL=104	4.1.7	10.04	_	7.044	?	74.8	70.1	۲.	7.0	00.0	7.046	0.0	1.05.4	, o		74/7
AVS(+) AT PLEZK	- 45	10°04		 	105	97.0	4 a 4	P.	٠.٧	0.00	750.4	00.0	105.4			^*/^
449(-) At 41.52×	÷.=	A.00k		1.07	103	A7.0	030	6.10	٠.٠	c c c	** 644	č	1.05	10.01		^>\
AVS AF SVSV. PLETON	5.15	* 1177		- 40 -	ď	78.0	15.1	٠٠.	0.0	00.0	1.2.1	٠,٠,٠	105.4	500		>> >
AVS AT SV SV. DL = >4	ď.	171.			7.0	6.5.5	₽4.3	477	٠,٠	00.0	۲.۲	c c	1.5.X	501		^*/^
90(+) AT 20V,+20V	₹.	25.0		5.14	₽	77.4	۷۰٬۰	1.7.1	1.50	00.0	7.57	000	0.05	75.0		S::/>
99(-) AT 201,-201	11.5	٠.٢		3.73	2	\$0°3	11.7	, , ,	1.50	60.0	5.11	17.4	C	25.0	7.70	V V
NOTES: 1/ * Excludes population outside of	ludes	sepula	tion c	vutsid	e of	low	rei	4/ The	, % Fa	11 for	-	and SR on this	20	4	toblo o	
40.44	407	•			•						ပ္ပ ်	, dire		6711	a arns	918
		_							. Vaii	not valid since all	e all	device	e types		are compared	ared
,						į		S	type	to type Ol limits.	nits.					
2/ % fail values	l value	۱۱ دد	5% are circled	cfrc	led	$\left(\right)$										
						•	•	5/ The	re ts	00	aria i A	fail	linit	for	There is no maximum fail limit for eath and	7
3/ Figure of		erit d	merit definitions:	ions:			•		Slew rate	4		1			24411 8	2
o il					٠			•	3	•						

Table 2-9. -55°C Statistical Summary For LF155A Series Devices.

LO - FM = Z - 10w 11mit

HI - FM = Figh limit

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VPO(-0-1 A) 3575v	4	7.97	1 4 d 7	=======================================	- 60	ر. د. د.	40.0		5.50	- c - C - T	; ;	7.04	٠, ۲	c . c .	1.47	:
VID(+C4) AT 54,-157	-3. 34	٨. ٣٠	50.4	;·	٠.		٠ • •	ŕ.	05.7	c • • • • • • • • • • • • • • • • • • •	1.70	(B • t	·.	٠,٠	1.42	>
	-11.13	, L	F. F.	÷.	<u> </u>	ر. د د د د د د د د د د د د د د د د د د د		? }:	1,5.	· · · · ·	7 7	۲, ۵۶	Ç.	٠ <u>٠</u> ٠	. a .	>
VINCOCO) AT Sv 5v	: 1 : 7 :	\$.05	-74.11		<u>2</u>	47.7	و		. 5.5	٠.٥	٠ ٤	7.04	٠	10.	1.00	^
110(-C*) AT 35v5v	-1.46	10.4	RIO.	¥: .~	701	ر. د د د د	c.	? •	*0.16	¥c.07-	4.54	00.0	¥. *	· ·	24.	4
TIDIOCAL AT SV 85V	-2.17	14° 1K		` <u>`</u>	2	0.84	٠,	<u>.</u>	*(°C*-	*0 ° 0 ! •	· · ·	٠,	¥.	*C** UT:	17.4	₹.
110(0(4) 41 20V, -201	41/4.5-	1.7	505	1.77	<u>-</u>	1.10	÷.	<u>.</u>	*V*(?-	40.06-	٠ <u>.</u>	٠ ٠ ٠	· (~	¥. * . *	. · · ·	8 0
110(+C*) AT 50, -25v	**	7	٠,٥٥	1.744	2	= 40	- 00	÷.	* · · · · · · · ·	10.01-	11.5	() • (¥0.	¥ 0 * C *	? · · ·	•
**************************************	->24	***	7.0.2	1.45	192		٠ ٢	<i>:</i>	-13.34	*C*01+	۲۰۰	٠, ٥	אַט•ּור	¥0.04	٠,٠٠	7.
**************************************	· · · ·	3. CK	13.44	1.7	1.	۲٠٠	÷.	÷.	-1.5.74	-10.01-	٠,٠	٠.	A 1. 8	¥	c .	•
ATTHEORY) AT 20V, -20V		17.74	P. F.	10,74	301	- -	÷	ر. د	¥C.01.	-10.0K	. 7.	, c c	,	ć .	4	40
THE COURT OF STREET	-51.7	71.2K	, n c	10.54	1,0	1.50		Ę.	¥	10.04	- ·	> . c d o	5.0 ¢ 0.4	40°64	1.01	4
-1114(+C4) by 15c5c	- 8 15.	47.4K	5.21.	7.144	133	1.50		ź.	-10.14	*10.01	۲۰۱۶		* c	,	4.24	٥
135-145 18 (mJ+)HII-	٠. ٢	5h. 4K	12.7.	11.4x	101	۲۰۰	07.1	ć.	-1.), 24	10.01	7.	7.040	10.04	ć C	71.7	٠,
FILM (GEV) AT POVE-		40.04	4.154	77°°°	<u>^</u>	35.1	c.	<u>.</u>	-10.04	10° JE	1.72	> • c 40	۶ ۰ ، ۲	# D . C .	To . 7	•
-11H(+C+) A1 SV25V	٠.١٧	4 H . LX	4 · * ·	10.1	~	1.50	÷	<u>.</u>	10.01	-10.04	~ ~	7 ° C R (7	¥ (°	¥ • O *	7.00	7 6
ADSOL AT TOUGH	74.9	1 47.	122.	- 0 0	<u>-</u>	1.5.	ς. α 0	•	ر. د .	ر. د	3.74	ر ، • د	, CD.	151.	1 A O .	ii.
101-102 18 casa-	14.9	-	-10.	5.00		٠٠٠	٠.	4 0 (44	C. V.	0.05	۲۰۰	ζ.	×., .	15,	170.	T.
AUC-PAUC IN END	74.5	124.	* 00	¥.	102	- 70	ت. ده	, .	ع آ.	ر• ، ک	٠٠,	00.0	¥	150.	716.	a c
V-401(+) AT 201,-201	10.7	1.1	1.4.0	317.	<u>-</u>	1	÷		c •	c	12.7	c c	٠,۲	٠ د د	C 05	ž
V-ADI(-) AT 20V,-26v	7:	, e	c. 7 [-	557°	0 C 1	1.7	- ÷	Ę.	, OC.	0.06-	. 27.0	6.	ر د د د • ۲	ر . د	,	>
1364) 41 150,-150	H . C .	00.0	-14.7	. 4	2	c . 10	÷.	<i>:</i>	6.65	-40	¥.	c c	¥ 0 C *	0,00	29A.	5
178(-) AT 154,-15V	۲. ۲	= = = = = = = = = = = = = = = = = = =	٠.٠	۶.	207	c .	٠ •		¥00°.	9.49			٠,	c .	7.8.7	4
ICC AT 15v15v	۶. <u>۲</u>	٠.٠	1.7.	7.	<u> </u>	97.1	c.	:	:	ē.	:	4.04		٠,	7.000	4 ~
AVUP AT JETCE		4.4	٦٠,4	~~~	=		95.1	· .	-		۲. ۲.	6	٠,	`. `	# # # # # # # # # # # # # # # # # # #	>
-VIP BT PLEIDA	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	£. x	a. ۲.	A.X.	101	٠.	0	•	- 5.0.5	٠,٠	>.1,₹	> . c d 0	٠.٠	٠.	* 3 . *	د
* THE BE # 1	15.7	۲. ۲.	1 7 . H	2 4.1	-	C .	c :	3	c	٠.٠	۲.	c C	()	ت . د ک		د
TO THE PERSE	~ ~ ~	7.5	-17.4	7 70	č	C .	•	6.	007	. 20.		· ·			2.5	>
	71.	7.504	1.75*	1.474	7	9.0	× .	- -	. ·	C 0 .	- -		٠ -	¥	•	7
4V9(-) AT 4LEID4	<i>-</i> :	10.04	. 0 .	1.804	~	₽.y. ♣	M	; (٠.	0.0	٠.	ر. د • د	100	,	٧.٧	**/>
AVS(+) AT PL=>+	17.2	7.50#	1.41	1.574	6	\ ¥ 7	÷.		٠.	0.0	<u>-</u>	ر د •	1.5°	10.01	65.7	,,,,
	3.1.5	¥0.	1.674	¥	27	٠. ج		7	٠.	c c		c	¥.		9	> > > > > > > > > > > > > > > > > > > >
	- · · ·		==		=	- č	1,1		٠ -	ć .	3°07/	c .	Y	1.034	740	>>
TELEVASTINE AT SAT	۲۰۰۲		100	1.14	÷.	27.5		÷:	c .	C .	,	ξ.	¥.		. 20	; ;
34(+) AT 20V20V	A	7""	10.7	~ · ~	£		۲.,		٠. د	ć .	٠.	٠, در	٠.٠	· ·	۲.	V V
2001-200 DE (1)75	٠ ۲	٠,٠	0.0	¥ .	45	, c	47.1	÷.	.50	٠.0	٠.٠٠ ٠	<u>د</u> .	÷.	· ·	÷.	V:

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits. NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values \geq 5% are circled \bigcirc

3/ Figure of merit definitions:

5/ There is no maximum fail limit for gain and slew rate.

LO - FM =
$$\overline{X}$$
 - low limit

O

HI - FM = High limit - \overline{X}

Table 2-10, 125°C Statistical Summary For LF155A Series Devices.

LF155/6/7 PARAMETER DISTRIBUTIONS & LIMITS

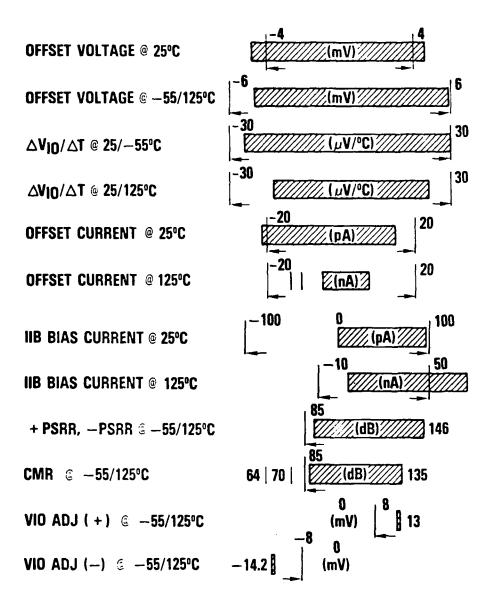


Table 2-11. LF155/6/7 Data Distributions.

LF 155/6/7 PARAMETER DISTRIBUTIONS & LIMITS

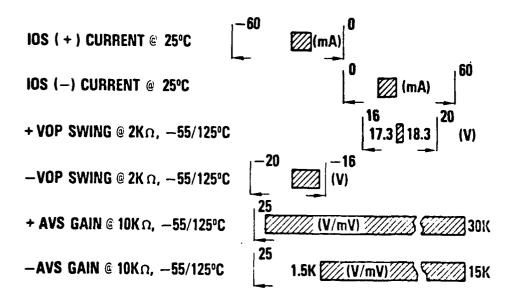
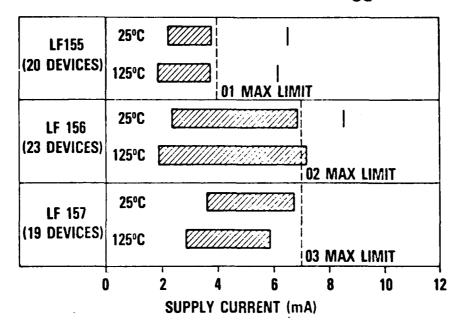


Table 2-11. LF155/6/7 Data Distributions (cont.).

SUPPLY CURRENT vs DEVICE TYPE @ ± VCC = ±15V



SLEW RATE RANGE vs DEVICE TYPE

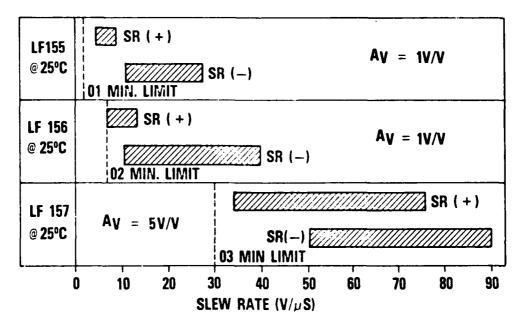


Table 2-12. LF155/6/7 Supply Current & Slew Rate vs Device Type.
II-43

 $A_V = 1 V/V$

		VENT	VENDOR CODE A	≪		-	VEND	VENDOR CODE B*	**			VEND	VENDOR CODE B	<u>م</u>			UNITS
Parameter Symbol	Conditions	12	13	. 2	2	9	8	16	6	93	76	83	98	87	80	89	
18(tr)	ve 05v	777	8	×	53	4.7	67	57	41	67	63	87	8	94		97	:
	ve. = 0v	87	88	9/	7,9	63	25	87	7,	56	87						
TR(os)	vo = .05v	43	42	38	3	47	88	35	35	33	36	36	36	38		77	ы
	vs. = 0v	97	88	8	*	36	33	31	¥	59	32						
SR (+)	vo = -5v													•		(
	TO + 5V	7.5	5.0	11.5	12.0	11.0	9.0	8.5	11.5	7.0	0.0	o.	?	0.	3	2	
SR (-)	ve - 5v	9	:		12.0	•	9 5 17 0 17 5	17.5	0 82	13.5	15.5 17.5 13.5	17.5	13.5	0.61	20.5	19.0	v/v
	TO + 5V	2.61	2.31	3.6	2	;	?	<u>:</u>							 		
	ve - 5v																
5	TO + 5V	90	850	1000	8	1200	800	3.5	800	8	800	1300	1250	1000	8	200	2

TABLE 2-13. LF155 Dynamic Data @ 25°C.

* Lr155A

 $A_V = 1 \text{ V/V}$

CINII	153	30	34	2 77	37	18.0 V/us	-	28.0 V/us			1100 ne	
	152	* 	13	5 7	%	14.0	1	26.0 29.5 29.0 20.5			1300	
DE E*	151	38	z	7	390	16.0 24.0 25.0 14.0		29.0			1100	
VENDOR CODE Serial No.	150	39	32	97	0,	24.0		29.5			1000	
VEN	149	33	07	77	36	16.0		76.0			1100	
:	38	42	77	87	390	10.5		0 61			1300	
	37	45	9,	97	- 3¢	10.0		78 5			1200	
ODE A	36	75	77	77	390	9.5 10.5 10.0 10.5					1250	
VENDOR CODE Serial No.	33	7,7	(7)	87	380				200		900 1100 1200 1250	
Y. S.	34	4.5	8	97	36	9.5					1100	
	134	35	35	77	38	16.0					900	l
	133	39	7	4.2	-9¢	15.0 17.0 10.0			?•		1100	l
DE B*	132	35	37	\$	38	17.0			31.5		006	
VENDOR CODE Serial No.	131	28	38	77	37	15.0			2.5		8	
VEN	130	28	33	1.7	39	17.5			?		<u></u>	
	Conditions Ay = 1 V/V	vso. = ov	vo. • .5v	ve ov	vo = .5v	V2 = 07 V2 + 07		. AS- = OA	10 + 24	ve ov	T0 + 5V	
	Parameter Symbol	TR (tr)		TR (ce)		SR (+)		SR (•)		5		

* LF156A

TABLE 2-14. LF156 Dynamic Data @ 25°C.

A. = 5 V/V

		VE	VENDOR CODE Serial No.	ODE D			VEN	VENDOR CODE Serial No.	No.			VE	VENDOR CODE Serial No.	ODE B			11.62
arameter Symbol	Conditions A/V = 5 V/V	09	19	62	67	89	69	02	ıı	72	73	82	79	80	81	82	
TR (tr)	v20. = 0v	270	097	290	290	260	290	300	280	310	290	240	260	250	260	280	8 0
	vo • .s																
TR (08)	ve05v	0	0	0	0	С	C	0	С	0	C	0	C	0	ာ	0	9.2
	vs. = 0v																
SR (+)	VO = -5V																
	TO + 5V	95.0	80.0	75.0	0.07	75.0	75.0	65.0	95.0 80.0 75.0 70.0 75.0 75.0 65.0 80.0 70.0 75.0 80.0 65.0	0.07	75.0	80.0	65.0	80.0	80.0 50.0	75.0	sn//
SR (-)	ve = 0v																
	TO + 5V	0.06	85.0	95.0	80.0	75.0	85.0	85.0	90.0 85.0 95.0 80.0 75.0 85.0 85.0 110.0 90.0		95.0	95.0	0.08	95.0 95.0 80.0 85.0 85.0	85.0	90.0	V/us
5	v2- • 0v																
	TO + 5V	450	95,7	95,7	250	200	007	300	8	007	300	550	99	8	650	8	.
						Ì		1							•		•

TABLE 2-15. LF157 Dynamic Data @ 25°C.

2.5 Discussion

On a parameter by parameter basis, a discussion of the device characteristics follows:

2.5.1 Input Offset Voltage (V_{IO})

LF155/156/157 Family

This family of devices had very good yields in passing the $\rm V_{10}$ tests over the common mode voltage and military temperature range. The screening limits for these devices were \pm 4 mV and \pm 6 mV at 25°C and over the military temperature range respectively. These limits were subsequently expanded to 5 mV and 7 mV respectively, as part of a decision to include the LF155A series op amps as separate device types with low offset voltage in the slash sheet.

In early 1979 a GIDEP (Government Industry Data Exchange Program) alert was issued on Vendor Code E LF155 devices became of high offset voltage drift with time (greater than 10 mV). The vendor said that the problem was caused by contamination during the ion implant and cleaning procedures, which resulted in a surface inversion condition. A 168 hour burn-in test at GE Ordnance Systems on the LF155 series group from vendor codes A, B, C and D revealed a maximum offset voltage shift of less than 0.8 mV. Most devices had less than 0.3 mV of offset drift.

A related problem is with short term power turn-on offset voltage shift. The 1/15/79 edition of Circuit News reported on this phenomenon. Some sample testing was also done at GE Ordnance Systems without finding any devices having this problem.

LF155A/156A/157A Family

The test yields of the LF155A series devices to the tighter limits of 2 mV/2.5 mV were considerably lower than those for the non-A devices. Tables 2-8, 2-9 and 2-10 show this information in terms of percent fail high and percent fail low. Overall yields at 25°C , -55 C and 125°C were approximately 80%, 66% and 92% respectively.

2.5.2 Offset Voltage Temperature Sensitivity (\therefore V₁₀/ \land 1)

LF155/156/157 Family

 $\Delta V_{IO}/\Delta$ T is a very important parameter for applications having tight error specifications over a wide temperature range. Offset adjustment can not compensate for poor offset voltage drift. The user's only guarantee is to test for this parameter to screen out inferior devices.

With limits of \cdot 30 uV/ C, the non-A's had yields of 94% and 97% for the cold and hot excursions from 25°C.

LF155A/156A/157A Family

Even though the manufacturers catalog limits of : 5 uV/°C were relaxed to : 10 uV/°C, the test yields for the A series devices were 43% and 90% for the cold and hot Δ V $_{10}/\Delta$ T measurements, respectively. It was later determined that the LF155A devices from vendor Code B were not prescreened to truly certify them as A's. Follow up tests with vendor Code B indicated that good yields could be achieved with the = 10 uV/°C limits. From 25 C to 125°C V $_{10}$ is allowed to increase from \pm 2 mV to \pm 2.5 mV. This corresponds to an end point shift of 500 uV/100°C = 5 uV/°C.

2.5.3 Input Offset Current (I_{IO})

Since Bi-FET op amp offset current is the difference between the two input leakage bias currents, it is very small and also difficult to measure. Only the zero common mode voltage condition is covered by the /114 specification. Test yields were 93.5% and 64% for the non-A's and A's respectively, against the · 20 pA limits.

Most of the failures were traced to 156 A's and 157 A's from Vendor Code E. Test yields were worse for the "unspecified" -15V common mode condition because of front end matching considerations. At + 15 V common mode the test yield is better because the acceptance limit is raised to compensate for the higher input bias current.

2.5.4 Input Bias Current (+ I_{IB} , - I_{IB})

Figures 2-8 thru 2-ll show the sensitivity of input bias current to common mode voltage and power supply voltage. The slash sheet specification is based on \pm $V_{\rm CC}$ = \pm 20 V because of a precedent established with previous military op amp specifications and a desire to maintain standards for comparison.

It should be obvious from these figures that if low I_{1B} is a necessary application requirement, the supply voltages should be no higher than 15 V. Also with the lower supply voltages, the common mode voltage range is more evenly centered about zero. As the common mode voltage approaches the negative power supply voltage, the P-N junction between the gate and channel of the input J-FETs becomes forward biased and forward current is pulled out of the gate. The input common mode voltage corresponding to this "forbidden" condition is within three volts of - V_{CC} .

Increasing the common mode voltage in the positive direction causes reverse leakage current to flow into the J-FET gate terminals. The common mode voltage range over which the input J-FETs are technically in the leakage mode varies according to diffusion characteristics, geometry and minority carries concentrations. Also the leakage current is almost independent of reverse voltage.

The typical diode shape increase in bias current with common mode voltage occurs as the junction enters the avalanche or zener voltage range. Series resistance prevents the classical zener constant voltage characteristic from occurring.

Process differences among the device manufacturers cause the bias current vs common mode voltage characteristics to vary accordingly as can be seen in Figures 2-8 thru 2-10. Since the input bias current is J-FET gate leakage it is not surprising that this current is highly temperature sensitive. Typically, leakage current doubles for every 10°C rise in temperature. Figures 2-12 and 2-13 show this effect.

The test yields to the /114 specification limits were good except for the following:

1. Vendor Code E. LF155A series devices incorporating bias current compensation had a yield of only 16.6% for the negative common mode low limit of - 100 pA. Bias current compensation uses negative PNP collector current to cancel positive J-FET gate current. At the negative common mode condition an over cancelled situation is more likely to occur. The JC-41 Committee has not asked for relief on this limit.

- 2.5.4 Input Bias Current (continued)
 - Venc'or Code C. LF155 series devices had a yield of 30.7% for the 125°C input bias current limits of 50 mA and 60 mA at the zero and positive common mode conditions respectively. No relief has been asked for this limit.
- 2.5.5 Power Supply Rejection Ratio (+ PSRR, PSRR)

All of the devices had good yields in meeting the $85~\mathrm{dB}$ minimum limit.

2.5.6 Common Mode Rejection (CMR)

Good yields were obtained in meeting the 85 dB minimum limit. This parameter is calculated from the $\rm V_{IO}$ change over the input common mode range. Consequently, there is a close relationship between $\rm V_{IO}$ and CMR failures.

2.5.7 Input Offset Voltage Adjustment (V_{10} ADJ (+), V_{10} ADJ (-)

Traditionally, the requirement for offset voltage adjustment is that it be capable of driving the input offset voltage one millivolt beyond the minimum and maximum limits of offset voltage. All functional devices far exceeded this requirement with typical values of 13 mV and - 14.3 mV for the positive and negative adjustments respectively.

2.5.8 Short Circuit Current (I_{OS} (+), I_{OS} (-))

The instantaneous short circuit current was considerably less than the 50 mA maximum requirement. The short circuit current magnitude decreases with increasing temperature for both output drive polarities. If the output is commanded to be at the positive swing limit and then a short circuit is made between the output and ground or the negative power supply, the short circuit current I_{OS} (+), will be current limited by Q_A and R_1 in Figure 2-1. Accordingly, typical I_{OS} (+) = $\frac{V_{BEQ4}}{R_1}$ = $\frac{600 \text{ mV}}{R_2}$ = 24 mA. Since $\frac{\Delta V_{BE}}{\Delta T}$ = - 2 mV/C,

the self heating of the device and the output transistor, will cause the short circuit current to decrease by $80~\mathrm{uA/C}$.

Output short circuit protection can not be guaranteed over the full - 55°C to 125°C military temperature range.

2.5.8 Short Circuit Current (continued)

Under worst case conditions, the maximum internal junction temperature of 175°C will be exceeded at ambient temperatures far below 125°C. The following equations apply:

1.
$$P_D = 2 V_{cc} I_{cc} + V_{cc} - V_0 I_{os}$$

2.
$$T_J = T_A + P_D \theta_{JA}$$

where

 P_D = device dissipation (mW)

 V_{CC} = power supply voltage (V)

I_{CC} = power supply current (mA)

 $V_0 = \text{output short circuit voltage (V)}$

Ios = output short circuit current (mA)

 T_T = junction temperature (°C)

 T_A = ambient temperature (°C)

 θ_{TA} = device junction to ambient thermal resistance (°C/mW)

Under worst case conditions and a "warmed-up" short circuit current of 30~mA, the devices have the following maximum safe ambient temperatures:

Device Type	Maximum Safe Ambi	
01, 04	89.5°C	22°C
02, 03, 05, 06	76°C	9° C

$$*T_A @ T_I = 175^{\circ}C$$

Several 02 and 03 devices were subjected to sustained output to power supply short circuits for several hours without incurring any damage. The real margin of safety depends on the differences between worst case and typical parameters.

2.5.9 Supply current (fee)

supply current is one of the parameters which is different for each device type in the L.155 series tamily. The $\Gamma_{\rm ex}$ limits are well chosen for the device data distribution.

2.5.16 Output Without Swin, or one, - conf.

Maximum output voltage swing is generally well behaved with a tight histogram pattern and a mean value which is two volts or better than the specification limit.

2.5.11 Open Loop Voltage Cain (Ays (+), Ays (-),

But for one exception, the data distribution of open loop voltage gain far exceeded the minimum specification. Characteristically, the gain histograms have a scattered distribution. There were no wrong polarity gains, thus indicating better management of thermal effects than were observed on many good op amps during previous characterization studies. LF155A devices from vendor Code B had many gain tailures at -35 C. Vendor Code B test violds at -35 C were 50., 15 8, and 16.6 for their LF155A, LF156A and LF157A devices respectively. These same devices had respectable gains at 25 C and 125 C.

2.5.12 Slew Rate (So (+), SR (+))

Each of the six device types is characterized by a different slew rate specification. Within the non- α and α groups of devices, slew rate is traded off with supply current to offer the user three design options. In most cases negative slew rate was faster than positive slew rate by almost $2\pi 1$

LF155/156/137 Family

All of the devices had good yields to their respective specification limits, except for Lil56's from Vender code , which had α **e**lds of 22 and 0° at 25°C and 125°C respectively

L. 135A/156A/157A Family

With the exception of Vendor (pdc 1, 150, decrees, which has a cost pierd of 50, all of the data has well vithin the specification limits—the failed 150A devices would pass the 450 limits—(i.e. 7 M/us vs. 10 M/us)—compared with big clar .p amps, with the open mps have a much better combination of high slow rate and low input bias current.

2.5.13 (ransient response (is (tr), 1s (os))

with a closed loop goin of LV/), the transfent response data of the LCL/) and LCL/b devices was significantly faster than the initial 10-41 committee recommended limits.

Also the 6x157 devices at a closed loop gain of 5 V/V were slower than the 40-41 Committee recommended limits. The data and limits are summarized below:

Device Type (AV	TR	(tr) ns)	Limits ! TR(() (') (min)!	os)	(r	(tr) is)	,	(OS)	Sample Size
Li'155 + ly/y		300		40	41	55	33	47	15
LF156	_	200	_	40	28	45	42	48	15
LF157 a 50/V	-	100	:	40	. 240	310	0	0	15

In order to resolve the differences between the recommend limits and the data, a second referee circuit was built and several devices were tested again. The new data correlated with the original data.

After verifying that the data matched, the sensitivity of the data to the circuit components was investigated. Not surprisingly, the feedback capacitor has a dominant effect. For instance a change from 10 pf to 18 pf caused the overshoot of an LF156A to decrease from 44/ to 32%. Figure 2-16 shows the typical response of an LF155 and an LF156 device. The high TR(OS) overshoot failure rate was resolved by modifying the test circuit such that for $A_V = 1 \text{ V/V}$, $R_F = 0$. Normally closed K9 contacts in parallel with the 10 K JL resistor of Figure 2-4 reduces the D.U.T. overshoot by making the device less susceptible to parasitic capacitance at the inverting input. Typically, depending on the D.U.T's characteristics, a reduction of 10% to 20% in overshoot was achieved.

2. v.13 ranspert pesponse (centinged)

closed coop carn has a big cliect on the transient response of an $4\pi 157$ or can be seen in figure 2*17.

Rise time and overshoot changed from 15 nanoseconas and 130 to 250 nanoseconds and 0 , respectively, when the closed loop gain was increased from 1 V/V to 5 to V. In raising the closed loop gain, the open loop gain is reduced by 14 dB and the effect of the high frequency poles and zeros is greatly reduced.

The revised transient response specification limits are shown in Table 2--16

2.5.14 Settling Time (ts(+), ts(-))

Settling time as defined in the 7114 specification is a sampled large signal test for the time it takes the error voltage to settle within 0.17 of its final value. A phantom summing mode is monitored as shown in Figure 2-5 while the DUT is exercised to produce a 10 V output pulse. This summing mode voltage $V_{\rm N}$ is proportional to the error voltage difference $V_{\rm E}$ between the input and output voltage as shown below:

$$v_{N} = v_{1N} \frac{R_{F}}{R_{1} + R_{F}} + v_{0} \frac{R_{1}}{R_{1} + R_{F}}$$

$$v_{N} = v_{1N} \frac{R_{F}}{R_{1} + R_{F}} - (\frac{R_{F}}{R_{1}}) \quad v_{1N} (\frac{R_{1}}{R_{1} + R_{F}})$$

$$v_{N} = \frac{R_{F}}{R_{1} + R_{F}} \quad v_{E}$$

Thus for circuit gains of - 1 V/V and - 5 V/V, the null voltage is .5 $V_{\rm E}$ and .833 $V_{\rm E}$, respectively. For a 10 V output and 0.1% error, the corresponding null voltage thresholds are 5 mV and 8.33 mV at $A_{\rm V}$ = 1 V/V and 5 V/V respectively.

Figure 2-20 shows the dynamic null error voltage of several typical devices. The settling time is composed of a slewing interval and transient response interval, which depend on different parameters and conditions. For a given device the slewing interval is pro-

2.5.14 Settline fime (continued)

portional to the output step change, whereas the transient response interval is dependent on the damping ratio of the device in the test circuit.

The circuit chised loop lain has a big effect on both the slewing interval and the transient response interval. Depending on how the response oscillations dampen, the difference between 0 1/ and .01 settling time can vary from a fractional part of cycle to several cycles.

The relationship between the data and the proposed limits is tabulated below:

Device Type	Data ts in	≄ 25 C (ns)		/11 ts in	4 A (ns)
Αγ	(min)	(max)	Sample Size	(min)	(max)
LF155 @ 1v/v	700	1300	15	-	1500
LF156 @ Iv/v	900	1300	15	:	1500
LF157 @ 5V/V	300	650	15	-	800

2.5.15 Noise (N_I (BB), N_I (PC))

Broadband and pop corn noise was measured with a Tektroniks Type 577 curve tracer. Typical data displays are shown in Figure 2-22.

Broadband noise was measured with a source resistance of 50 Λ and the observed peak-to-peak readings were divided by six to yield Gaussian rms values.

This factor of six is used because op amp noise voltage is random and has a normal statistical distribution. One of the properties of a normal Gaussian distribution is that the ratio of the peak-to-peak value over the rms value is six with a probability of 99.7%.

2.5.15 Noise (continued)

The data is summarized as follows:

Broadband Noise (u \rms)	Bara Frequency
0.3 0.7 0.8 1 0 1 2	1 5 3 10 1
1.3 1.7	1

Total: 24 data values

The data distribution is conservatively within the $10\ u$ Vrms maximum limits of the /114 specification.

For the popcorn noise test only one device had an observed "pop" of 10 u Vpk. The remaining 23 devices had no trace of popcorn noise.

2. ... Bors-it circuit symination

After the initial characterization data was taken, sixty non-A devices were burned-in using two different circuit configurations. Twenty-eight devices were exercised in the original voltage follower circuit which uses a 2000 ohm load. During this 168 hour burn-in test, the input was changed from + 5 V to - 5 V after approximately half of the time had elapsed. The remaining 32 devices were exercised on a new simplified circuit which has the inputs grounded and the outputs open. Maximum supply voltages of 22 VDC were applied to these devices, whereas only 20 VDC was applied to the first group. The two sample populations were chosen such that they equal representation with regard to vendor and date code.

At the conclusion of the 168 hours, 125 C test, the devices were cooled down before power was removed. The serialized devices were again tested on the S-3260. The following observations were made after comparing the before and after test data:

 For both test circuits the post burn in data total failures did not exceed the total pre burn-in tailures.
 In other words good devices, in general, are not harmed by either test circuit.

2.5.16 Burn-in Circuit Evaluation (cont.)

2. Quite often on particular devices pre burn-in failures did not appear at post burn-in. These were mainly I $_{\hbox{IO}}$ and $1_{\hbox{IB}}$ technical limit failures.

It was concluded that the new simplified burn-in circuit was equally effective with the old standard test circuit. Subsequently, it was recommended that the supply voltages be reduced to τ 20 V and the pin 5 offset adjust pin be a marking to τ $V_{\rm col}$.

2.6 che lastens and Recombedderens

204 LF155 series op amps were tested on GEOS' S-3263 to characterize their electrical parameters. Sampled bench test data was taken to characterize noise and some of the dynamic electrical characteristics, which could not be tested on the S-3263. It should be noted that the electrical characteristics are oriented toward automatic procurement testing. With the exceptions of input bias current, input offset current, and output short circuit current, the effects of device self heating will not cause the procurement values to differ from application values.

In order to minimize input bias currents and device power dissipation it is recommended that the power supply voltages be kept no higher than $15\ V$. Although these Bi-FET op amps are guaranteed to operate at 125 C ambient temperature, high temperature operation will cause the benefits of low input bias currents to be lost.

The LF155 series of Bi-FET op amps have several advantages over bipolar devices including a more optimum combination low bias current and high slew rate plus the ability to drive high capacitance loads.

Tinal recommended electrical specifications for the generic LF155 series op amps in MIL-M-38510/114 are shown in Table 2-16.

L-		$V = V \cdot V$ and it is the $V \cdot V = V \cdot V$		Limits		<u>,</u>
Characteristics	Symbol	ec i	Device	Min.	Max.	Units
Input offset	01,0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	04,05,06	1 I 61 70	2	mV mV
		$V_{CC} = 20 \text{ V}$ $V_{CM} = 15 \text{ V}, 0 \text{ V} -55 \text{ C} \xi T_{\Lambda} \xi + 125 \text{ C}$	04,05,06	-2.5	2.5	η η η
Input oilset voltage temperature sensitivity	Δ ^V 10 Δ ^T	$\frac{V_{CC}}{V_{CM}} = 0.0$	01,02,03 04,05,06	-30	30	uv/ c
Input offset	01]	$V_{CC} = 20 \text{ V}$ T _J = 25 C	a11	-20	20	pA
current	2	$V_{CM} = 0 \text{ V, } t \le 25 \text{ ms} $ $T_J = 125 \text{ C}$	a11	-20	20	L'A
Input bias	+ 11%	$V_{CC} = -20 \text{ V}$ T ₁ = 25 C	all	- 100	3500	pA
current		+ 15 V, t \ 25 ms	all	-10	09	Yu
	- 418	$V_{CC} = 15 V \qquad T_{J} = 25 C$	all	- 100	300	рА
	1/1	$V_{CM} = + 10 \text{ V}, t \le 25 \text{ms T}_J = 125 \text{ C}$	a11	-10	20	٧'n
	77	$V_{\rm CC} = 20 \text{ V}$ $\Gamma_{\rm J} = 25 \text{ C}$	all	-100	100	рЛ
	3/	'≤V _{CM} ≤0 V, ms	all	- 10	20	150
Power supply	+PSRR	$+ V_{CC} = 10 \text{ V}, - V_{CC} = -20 \text{ V}$	all	85		dB
	-PSRR	$+ V_{CC} = 20 \text{ V}, - V_{CC} = -10 \text{ V}$	a11	36.5	•	dB
input voltage common mode	CMR		a11	ź.	1 1	dB
re ject 10n 4/				+		

Sec footnotes at end of table.

Table 2-16. Proposed Electrical performance Characteristics For ML-M-38510/114.

i	-	-					ļ
Characteristics	Svmbo1	Conditions (V _{cc} = unless otherwise sp	= 20 V specified)	Device	limits Min. M	its Max.	Units
Adjustment for input offset	γ ₁₀ ADJ(+)	$V_{\rm CC} = -20 \text{ V}$		all	∞ +		Λm
voltage	V10 ADJ (-)	V _{CC} = 20 V		a11		∞ -	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
Output short circuit current (for positive output)5/	(+) SO ₁	V _{CC} = 15 V t < 25 mS (Short circuit to ground)	round)	a11	- 50		mA
Output short circuit current (for negative output)5/	(-) SO ₁	$V_{CC} = 15 \text{ V}$ t $< 25 \text{ mS}$ (Short circuit to ground)	(round)	a11		20	A.M.
Supply current	၁၁	V _{CC} = . 15 V	TA = -55° C	01,04		9 =	
			$T_A = +25^{\circ} C$	02,03,05,06		77	щĄ
			$T_{A} = +125^{\circ} C$	01,04 02,03,05,06		77 ~	
Output voltage	$^{ m V}_{ m OP}$	$V_{CC} = V_{CC} \times R_{L}$	= 10 K A.	a11	16		=
(may Timan)		$V_{\rm CC} = 0.20 \text{ V}, R_{\rm L}$	= 2 K A	all	15		_
en loop voltage iin (single ended)	Avs (~)	$V_{CC} = 20 \text{ V}$ $R_T = 2 \text{ K} A$	T _A = 25°C	all	20		
/9		$V_{00T} = 15 \text{ V} -55^{\circ}\text{C}$	°C £TA £+125°C	all	25		\m / \
Open loop voltage gain (single ended)	Avs	$V_{\text{CC}} = + 5 \text{ V}$ $R_{\text{L}} = 2 \text{ K.} \Omega$ $V_{\text{Out}} = -2 \text{ V}$		all	10		\/m/\

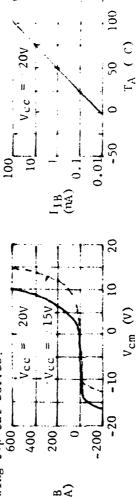
See footnotes at end of table.

Table 2-16. Proposed Electrical Performance Characteristics For MIL-M-38510/114.

			= 20 V	. •	Limits	its	.
Characteristics	Symbol	unless otherwise	specilied)	Device	Min.	Max.	Units
Transient response rise time	TR(tr)	$V_{CC} = 15 \text{ V}$ $R_{L} = 2 \text{ K}$ $C_{L} = 100 \text{ pf}$	$\Lambda_{V} = 1$	01,04 02,05	1 1	150	s u
		See Figure 8	$A_V = 5$	03,06		450	
Transient response	TR(0S)		$A_V = 1$	01,02,04,05		0 7	
overshoot			$A_V = 5$	03,06		25	
Slew rate	SR(+)	ľ	$T_A = 25^{\circ} C$	01	2		<u> </u>
	and	V _{CC} = 15 V		07 04 07	ຸ ຕ `_		
		sec Figure 8		0.5	10	1 1	V/us
	SR(-)		$T_{A} = -55 \text{ c}, 125 \text{ c}$	01	1	;	
			4	02	نک ر د	:	
				77 022	1.5	1 1	
		7 5 × N1.7	T = 25. C	03	30		
		= ⁻ 22		90	0,7	•	
		3 - N					
		Sec Figure 8	$T_{A} = -55 \text{ c}, 125' \text{ c}$	03	20 3.0	t	
					,		İ
Settling time	ts(+) and	$V_{CC} = 15 V$ (0.1) error) F. = 25 C	= ^ ~	01,02,04,05	i i i	1 500	SC
	(-) s ₁	Sec Figure 9	$\Lambda_V = 5$	03,06		800	
Noise (reterred to input) broad- band	(88) ¹ N	$V_{CC} = 20 \text{ V}$ Bandwidth = 5kHz	TA = 25 C	a11		0	υVrms
Noise (referred to input) popeorn	N ₁ (PC)		$1_{A} = 25 \text{ C}$	a11		80	uľ.pk
	-						

Table 2-16. Troposed Electrical Performance Characteristics For MIL-M-38510/114.

Bias current is sensitive to power supply voltage, common mode voltage and temperature as sleen by the following typical curves: 75



Negative $I_{
m IB}$ minimum limits reflect the characteristics of devices with bias current componention. 2

CMR is calculated from ${
m V_{IO}}$ measurements at ${
m V_{CM}}$ = + 15 ${
m V}$ and - 15 ${
m V_{\bullet}}$ 71 Continuous limits shall be considerably lower. Protection for shorts to either suggly exists providing that T_J (max) ≤ 175 C. 2/

linear or positive over the operating range. These requirements, it needed, should be specified Because of thermal feedback effects from output to input, open loop gain is not graranteed to be by the user in additional procurement documents, **/**9

Table 2-16. Proposed Electrical Performance Characteristics For MIL-M-38519/114.

SUCTION III

ADJUSTABLE POSITIVE VOLTAGE REGULATORS

NH -M-38510/117

ADDICATA DEL MICATETTA VOLTACIE RECULATORA

MUL-M-38310/418

	TABLE OF CONTENTS	Page
	List of Figures	111-11
	List of Tables	- vi
3.1	Background and Introduction	111-1
3.2	Description of Device Types	111-2
3.2.1	Four-terminal Adjustable Voltage Regulators	111-5
3.2.2	Three-terminal Adjustable Voltage Regulators	111-6
3.3	Device Characterization	8-111
3.3.1	Automatic Test Development	111-8
3.3.1.1	S-3273 Test Adapter	8-111
3.3.1.2	Test Circuits and Procedures	111-8
3.3.1.2.1	VOUT, VRLINE , VRLOAD & VRTH Tests	111-9
3.3.1.2.2	$I_{\hbox{ADJ}}$ and $I_{\hbox{SCD}}$ Current Tests (Line & Load)	111-10
3.3.1.2.3	I_Q Test and $I_{CONTROL}$ Test	11-11
3.3.1.2.4	IOS, IPEAK and VOUT Recovery Tests	111-12
3.3.1.2.5	V _{START} Tests	111-12
3.3.1.3	Test Accuracies and Correlation	111-13
3 3.2	Bench Tests	111-15
3.4	Test Results and Evaluation of Data	111-15

111-15

(ABLE OF COMPLNES (cont.)

		Page
3 + .1	EMILITY Adjustable Positive Voltage Regulators	111-15
3.4.2	LM117K Adjustable Positive Voltage Regulators	111-16
3 4.3	LM137H Adjustable Negative Voltage Regulators	111-16
3.4.4	LM137K Adjustable Negative Voltage Regulators	III-16
3 4 5	Comparison of Data on 3-terminal Devices	III-17
3.4.6	Four-terminal Devices	III-17
3.5	Conclusions & Recommendations	III - 18
3.5.1	Test Circuits	111-18
3.5.2	Devices Under Test	III - 19
3.6	Bibliography	111-21

LIST OF FIGURES

Figure	Title	Page
3.1	Bandgap Reference	111-3
3.2	Adjustable Voltage Regulator with Protective Circuits	111-4
3.3	Block Diagram of 4-terminal Adjustable Positive Voltage Regulator	111-5
3.4	Block Diagram of 4-terminal Adjustable Negative Voltage Regulator	111-5
3.5	Block Diagram of 3-terminal Adjustable Positive Voltage Regulator	111-6
3.6	Block Diagram of 3-terminal Adjustable Negative Voltage Regulator	111-7
3.7	Voltage Regulator Test Adapter (Top View)	111-21
3.8	Voltage Regulator Test Adapter (Bottom View)	111-21
3.9	Positive Voltage Regulator Test Circuit For Static Tests	111-2
3.10	Negative Voltage Regulator Test Circuit For Static Tests.	111-25
3.11	evel Shift Circuit and Amplifier for VRLINE, VRLOAD &	111-27
3.12	RTH Tests. For itive Voltage Regulator Timing Sequence for $V_{\rm START}$ $I_{\rm OS}$ & $V_{\rm OUT}$ RECOV.	111-28
3.13	Negative voltage Regulator Timing Sequence for $\rm V_{STARI}$, $\rm I_{OS}~\&~V_{OUT}~RECOV$.	111-29
3.14	S-3263 Test System Differential Voltage Accuracy (Range Comparison)	1:1-30
3.15	S-3263 Test System Differential Voltage Accuracy (100 m V Range)	111-31
3.16	S-3263 Test System Differential Voltage Accuracy (1 Volt Range)	111 - 32
; 1 °	S-3263 Test System Differential Voltage Accuracy (10 Volt Range)	111-33
	- Ost test System Differential Voltage Accuracy	111-34

LIST OF FIGURES (Cont.)

Figure	Title	Page
3,19	Noise Test Circuit for Positive Voltage Regulators	111-35
3.20	Noise Test Circuit for Negative Voltage Regulators	III- 36
3.21	Ripple Rejection Test Circuit for Positive Voltage Regulators	III- 37
3.22	Ripple Rejection Test Circuit for Negative Voltage Regulators	111-38
3.23	Line Transient Response Test Circuit for Positive Voltage Regulators	III - 3 9
3.24	Line Transient Response Test Circuit for Negative Voltage Regulators	111-40
3.25	Load Transient Response Test Circuit for Positive Voltage Regulators	111-41
3.26	Load Transient Response Test Circuit for Negative Voltage Regulators	111-43
3.27	Oscillograph of LMl17H Load Regulation Measured at the Case	III - 45
3.28	Oscillograph of LM117H Load Regulation Measured 1/8 below Case	111-45
3.29	Oscillograph of LM117H Load Regulation Measured 3/8 below Case	III - 46
3.30	Oscillograph of LM117H Line Transient Response Test	III-46
3.31	Oscillograph of LM117H Load Transient Response Test	111-47
3.32	Oscillograph of LM117K Line Transient Response Test	111-47
3.33	()scillograph of LM117K Load Transient Response Test	III - 48
3.34	()scillograph of LM137H Line Transient Response Test	111-48
3.35	Oscillograph of LM137H Load Transient Response Test	111-49
3.36	Oscillograph of LM137K Line Transient Response Test	111-49
3.37	Oscillograph of LM137K Load Transient Response Test	III - 50
3.38	Alternate Test Circuit for Line, Load and Thermal Regulation	n III-51

LIST OF FIGURES (Cont.)

Figure	Title	Page
3.39	Average Line Regulation versus Temperature	111-52
3.40	Average Load Regulation (#2) versus femperature	11-52
3.41	Average Load Regulation (#1) versus l'emperature	111-53
3.42	Average Thermal Regulation versus Temperature	111-54
3.43	Average Adjustment Pin Current versus temperature	111-54
3.44	Average change of I_{ADJ} with Line Voltage versus Temperature	111-53
3.45	Average change of I_{ADJ} with Load (urrent versus Temperature	111-55

LIST OF TABLES

Table	Title	Page
3.1	Device Types Specified	111-2
3.2	Not (sed	
3.3	Test Conditions for 4-terminal Adjustable Positive Voltage Regulator (78MG)	111-56
3.4	Test Conditions for 4-terminal Adjustable Positive Voltage Regulator (78G)	III - 57
3.5	Test Conditions for 3-terminal Adjustable Positive Voltage Regulator (LM117H)	111-58
3.6	Test Condition for 3-terminal Adjustable Positive Voltage Regulator (LM117K)	111-59
3.7	Test Conditions for 4-terminal Adjustable Negative Voltage Regulators (79MG)	111-60
3.8	Test Conditions for 4-terminal Adjustable Negative Voltage Regulators (79G)	111-61
3.9	Test Conditions for 3-terminal Adjustable Negative Voltage Regulators (LM137H)	III - 62
3.10	Test Conditions for 3-terminal Adjustable Negative Voltage Regulators (LM137K)	111-63
3.11	Summary of S-3263 Test Adapter Accuracies	III - 64
3.12	Pos. Adj. Voltage Regulators - LM117H (25°C)	III - 65
3.13	Pos. Adj. Voltage Regulators - LM117H (-55°C)	I II-67
3.14	Pos. Adj. Voltage Regulators - LM117H (125°C)	111-69
3.15	Pos. Adj. Voltage Regulators - LM117H (25°C) Dynamic Tests	III-71
3.16	Pos. Adj. Voltage Regulators - LM117K (25°C)	III - 73
3.17	Pos. Adj. Voltage Regulators - LM117K (-55°C)	III - 75
3.18	Pos. Adj. Voltage Regulators - LM117K (125°C)	III - 77
3.19	Pos. Adj. Voltage Regulators - LM117K (25°C) Dynamic Tests	III - 79
3.20	Neg. Adj. Voltage Regulators - LM137H (25°C)	III-81

LIST OF TABLES (cont.)

Table	Title	Page
3.21	Neg. Adj. Voltage Regulators - LM137H (-55°C)	III-83
3.22	Neg. Adj. Voltage Regulators - LM137H (125°C)	III - 85
3.23	Neg. Adj. Voltage Regulators - LM137H (25°C) Dynamic Tests	III - 87
3.24	Neg. Adj. Voltage Regulators - LM137K (25°C)	III - 89
3.25	Neg. Adj. Voltage Regulators - LM137K (-55°C)	111-91
3.26	Neg. Adj. Voltage Regulators - LM137K (125°C)	111-93
3.27	Neg. Adj. Voltage Regulators - LM137K (25°C) Dynamic Tests	III - 95
3.28	Comparison of 3-terminal Device Data (25°C)	III-97
3.29	Comparison of 3-terminal Device Data (-55°C)	111-98
3.30	Comparison of 3-terminal Device Data (125°C)	III - 99
3.31	Electrical Performance Characteristics for Device Type 11701 (78MG)	III-100
3.32	Electrical Performance Characteristics for Device Type 11702 (78G)	111-101
3.33	Electrical Performance Characteristics for Device Type 11703 (LM117H)	111-102
3.34	Electrical Performance Characteristics for Device Type 11704 (LM117K)	111-103
3.35	Electrical Performance Characteristics for Device Type 11801 (79MG)	111-104
3.36	Electrical Performance Characteristics for Device Type 11802 (79G)	111-105
3.37	Electrical Performance Characteristics for Device Type 11803 (LM137H)	III-106
3.38	Electrical Performance Characteristics for Device Type 11804 (LM137K)	III-107

SECTION III

CHARACTERIZATION OF ADJUSTABLE POSITIVE VOLTAGE REGULATORS

MIL-M-38510/117

&

ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

MTL-M-38510/118

3.1 Background and Introduction

Prior characterization efforts for RADC have resulted in the development of slash sheets for Fixed Positive Voltage Regulators and Fixed Negative Voltage Regulators. These slash sheets, combined, specify regulators with \pm 5 Volts, \pm 12 Volts, \pm 15 Volts and \pm 24 Volts which survey showed are the predominate supply voltage requirements for either digital or analog circuits.

Several new innovative IC and hybrid devices incorporate precision circuitry and as such require low tolerance supply voltages. In addition, most large systems require a variety of supply voltages to provide power for digital circuits, analog circuits, display circuits, transducers, etc. The logistic problems associated with the variety of voltage regulators needed to power these devices can be greatly reduced by use os one of more adjustable voltage regulators together with a few standard value resistors.

Adjustable voltage regulators are available either as 4-terminal adjustable voltage devices or as 3-terminal adjustable voltage devices. Each of these styles has been characterized and is included on both of the slash sheets.

The following table shows the voltage regulators included in these specifications:

TABLE 3.1 Device Types specified.

Device Type	Output Volt Range	айс	Maximum Output current	Ne. of Jerminals		
11701	5v ≤ v _o ≤ 3	30 V	- 0.5 A	'.	11-5	78MG
11702	5/\≤\\%\≾\3		- 1.0 A	<u> </u>	~ 3	78 G
11703	$1.25v^{-1}v_{0} \le 3$		- 0.5 A	3	(1-5	LM117H
	1,25v≤v _o ≤		- 1.5 A	3	: 11-3	LML17K
11801	-30v≤v _o ≤ -	.5 \	0.5	•		7.9MC
11802	-30òá -		1.0 A	og .	10-3	7 9 G
11803	-37V ≤ V _o ≤ -		0.5 \	3	1:1-5	LM1371:
11804	-37v≤vo≤ -		1.5 A	3	· ()-3	LM137K
		i				•

3.2 Description of Device Types

The major physical distinctions between the various voltage regulators characterized for these two slash sheets are shown in Table 3.1—The major distinguishing features are: 1) voltage range and polarity, 2) maximum output current, 3) number of terminals and 4) case size. Whereas, the 4-terminal adjustable regulators are evolved from their fixed voltage—counterparts by deleting the two internal resistors used to set the output voltage and by bringing the error amplifier summing point out of the case, the 3-terminal adjustable regulators represent different approach in IC voltage regulator design and do not have 3-terminal fixed voltage counterparts.

All of these devices contain protective circuitry common to many of the available 10 voltage regulators. These circuits include a) output current limiting, b) short circuit protection, c) safe operating area protection and d) thermal shut down. In addition, the regulators included in these slash sheets feature "band-gap" reference voltage circuitry to fix and stabilize the output voltage. These reference voltage circuits are characterized by improved noise and long-term-stability. Generally, these characteristics are 10-100 times better than those found in standard avalanche breakdown reference voltage zener diodes. A simplified schematic of a band-gap reference is shown in Figure 3.1.

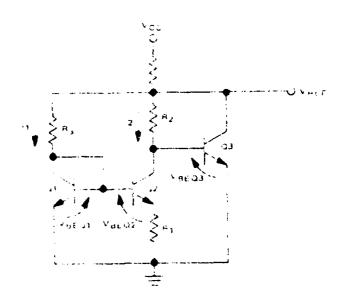


Figure 3.1. Bandgap relerence

In this circuit, two monolithic transistors operating at different collector current densities develop a voltage ΔV_{BE} , at the emitter of Q2. This voltage has the relationship: $\Delta V_{BE} = \frac{KT}{q} \ln \frac{(I1)}{(I2)}$ and the

temperature coefficient (TC) of this voltage is positive. When the voltage is amplified and added to the base-emitter voltage of Q3, which has a negative TC, the resultant output is:

$$v_{REF} = v_{REQ3} + \frac{R2}{R1} \triangle v_{BE}$$
.

By proper adjustment of the gain (R2/R1), the negative TC of V_{BEQ3} can be made to cancel the positive TC of ΔV_{BE} . The result is a voltage reference that has nearly zero temperature drift.

A simplified schematic of a positive voltage regulator showing the various protective circuits is shown in Figure 3.2. For the negative voltage regulators, circuit arrangement and performance is very similar.

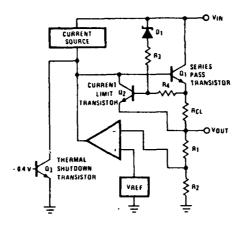


Figure 3.2. Ajustable Voltage Regulator with Protection Circuits.

The current limit circuit consists of Q2, R3 and R_{CL}. Resistor R_{CL} is in series with the output and carries the output current. Transistor Q2 is normally turned off; however, as the output current increases the voltage across R_{CL} increases and transistor Q2 begins to turn on. As Q2 conducts some of the series pass transistor base current is shunted around the transistor to the output and the current gain of the output circuit is effectively decreased. Thus, the total output current is degraded by the decrease in the output circuit current gain.

The safe area protection circuit consists of diode D1, transistor Q2 and resistors R3, R4 and R_{CL}. In the normal operating mode, Q2 is turned off and the current path for D1 is through resistors R3, R4 and R_{CL}. Since this is a high impedance path the diode current is insufficient to cause diode conduction. However, when the regulator is operating in a current limit mode, transistor Q2 is turned on, and diode D1 conducts through the transistor base-emitter junction. If the $V_{\rm in}$ - $V_{\rm out}$ voltage is greater than the breakdown voltage of the diode (6-8 volts), large base currents flow through Q2 and current limiting adjust to a much lower current level. Thus, the output short circuit current is greatly reduced as the regulator input voltage is increased.

The thermal shut down circuit consist of a transistor Q3 that is normally biased with is base-emitter junction voltage just below conduction ($V_{BE} \approx .4$ V). The thermal shutdown transistor is physically located next to the series pass transistor so that the two transistor temperatures are approximately the same. As the series pass transistor temperature increases, the required base-emitter voltage, necessary to turn-on the thermal shut down transistor, decreases. At temperatures around 150°C - 190°C, transistor Q3 turns on and the base current to the series pass transistor is shorted to ground. With these built-in protection circuits, the voltage regulator is virtually fail proof under the most abnormal operating conditions.

3.2.1 Four-terminal Adjustable Voltage Regulators

General block diagrams for the 4-terminal adjustable positive voltage regulator and the 4-terminal adjustable negative voltage regulator are respectively shown in Figures 3.3 and 3.4.

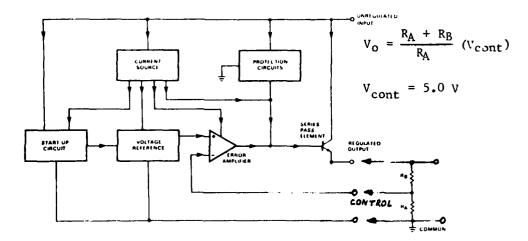


Figure 3.3. Block diagram of 4-terminal adjustable positive voltage regulators.

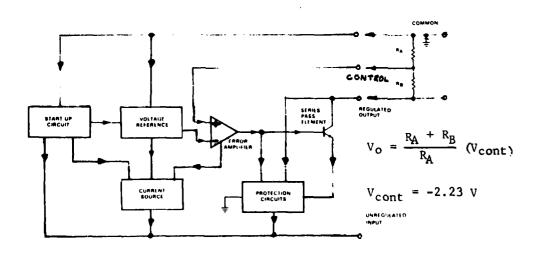


Figure 3.4. Block diagram of 4-terminal adjustable negative voltage regulators.

Both regulator circuits are made up of a) a start-up circuit to insure that the device is rapidly brought into regulation, b) a temperature-compensated voltage reference with a current source to eliminate the effect of the unregulated input voltage, c) an error amplifier that compares a fraction of the output voltage with the internal reference voltage, d) a series pass regulating transistor that controls the current output to the load, e) a series resistor and current limit to regulate the peak output current, f) a safe operating area circuit which operates with the current limit circuit to reduce the regulator's peak output current as the input voltage increases and g) a thermal shut-down circuit that turns off the pass transistor when its temperature exceeds 150°C - 190°C.

Circuit variations exist between each of the 4-terminal regulators as a result of the polarity differences and as a result of the maximum output current differences. A detailed discussion of the regulator circuits can be found in reference 1 listed in Section 3.6.

3.2.2 Three-terminal Adjustable Voltage Regulators

General block diagrams for the 3-terminal adjustable positive voltage regulator and the 3-terminal adjustable negative regulator are, respectively, shown in Figures 3.5 and 3.6.

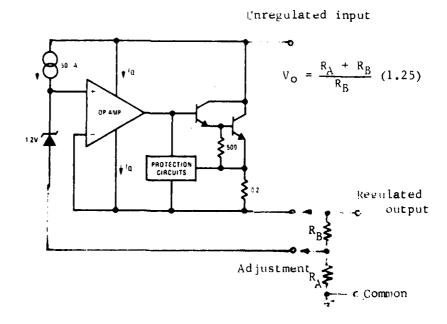


Figure 3.5 Block diagram of 3-terminal adjustable positive voltage regulators.

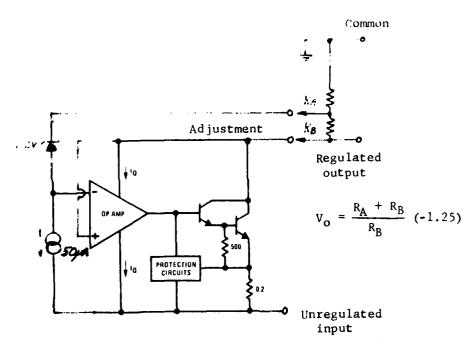


Figure 3.6. Block diagram of 3-terminal adjustable negative voltage regulators.

The 3-terminal adjustable voltage regulators vary markedly from the 4-terminal adjustable voltage regulators. The most outstanding feature of the 3-terminal regulators are that a) the quiescient current flows out of the regulator output pin instead of flowing out of the regulator adj (common) pin, b) the only current flowing out of the regulator adj pin is a low level current (50 uA) for the reference circuit, c) the error amplifier is a fixed unity gain amplifier and is therefore easily frequency stabilized, d) the voltage reference circuit does not require a special start-up circuit and e) large voltage stresses are restricted to the series pass transistor and to the on-chip current sources. The voltage $(V_0 - V_{adj})$ is a constant 1.2 volts. In addition, circuit refinements have resulted in improved thermal and load regulation. A detailed discussion of the regulator circuits can be found in reference 2 listed in section 3.6.

3.3 Device Characterization

Characterization of the 3-terminal voltage regulators was performed in two parts. The static tests that measure the d.c. parameters were performed on the Fektromix S-3203 Automatic Test System at -55° C, 25° C and 125 C. The dynamic tests including transient tests and a.c. tests were performed in a bench test setup at 2.%. The characterization effort for the 4-terminal voltage regulators was greatly reduced because of the similarity in design between the 4-terminal adjustable regulators and their 3-terminal fixed counterparts. The 3-terminal fixed regulators have been characterized in previous contracts to RADC and a report on this effort is provided in references 3 and 4 of section 3.6.

3.3.1 Automatic Test Development

Software was developed for the Tektronix S-3263 test system to provide for automatic testing of both the positive and negative adjustable voltage regulators. All static tests recommended by the JC-41 Committee and some GEOS added static tests were included as part of the software package.

3.3.1.1 S-3263 Test Adapter

The test adapter, shown in Figures 3.7 and 3.8, was designed to provide an interface between the DUT and the Test System. The adapter has the ability to test positive and negative, 3-terminal and 4-terminal, 1/2 amp, 1 amp and 1.5 amp regulators. This capability is achieved by using a separate plug-in carrier for each type of DUT. The carrier contains the input and output capacitors for the DUT, and plugs into the S-3263 main test adapter. In addition, the DUT protection diodes, and the current regulators and transistor used in the start-up circuit are on a separate 16-pin DIP carrier and are changed when the voltage polarity of the DUT to be tested is changed. Also the main current carrying power Darlington transistors are plug-in and can be changed from NPN to PNP or vice versa when the voltage polarity of the DUT is changed. Other plug-ins include load resistors and output voltage fixing resistors. In addition, the voltage measurement system has made extensive use of Kelvin test leads to insure that measurements are made at the precise point of interest.

3.3.1.2 Test Circuits and Procedures

The static test circuits developed for these characterization efforts were designed to permit regulator testing by either automatic test systems or by bench test instrumentation. Schematics are shown in Figures 3.9 and 3.10 and the test circuit set ups are listed in Tables 3.3 through 3.10.

The main DPT currents are carried by separate buses and are controlled by the automatic test system via the power Darlington transistor circuits. Through use of external power supplies, the adapter test circuits permit control of currents that are larger than the current capacity of the automatic test system.

The input power Darlington transistor circuit can force the value of the DUT input voltage and can be used to control it for testing a) output voltage versus input voltage, b) line regulation, c) short circuit current versus input voltages, d) start up, e) line transient and t) ripple voltage rejection. The output power Darlington transistor circuit can be used to force a current and measure the voltage or to force a voltage and measure the current. The circuit can be controlled for testing a) output voltage versus load current, b) load regulation, c) thermal regulation, d) short circuit current, e) voltage recovery, and f) load transient. The current-to-voltage amplifier is used to measure the milliampere and microampere currents for a) the standby current drain tests, b) the control current tests, c) the adjust pin current tests and d) the quiescent current test under a forced voltage condition.

3.3.1.2.1 VOUT, VRLINE, VRLOAD & VRTH Tests

All of the output voltage measurements use Kelvin sense leads and are measured differentially to the DUT reference point. The sense lead for the output voltage, line and load regulation measurements is terminated with a test clip lead. The clip lead is clipped to the DUT output lead 1/8 inch from the case. The voltage measurements are differentially compared to the output of a d.c. voltage standard and the difference voltage is amplified to optimize the best test measurement accuracy. The test circuit is as shown in Figure 3.11.

GENERAL ELECTRIC CO PITTSFIELD MA ORDNANCE SYSTEMS F/G 9/5
ELECTRICAL CHARACTERIZATION OF SPECIAL PURPOSE LINEAR MICROCIRC--ETC(U) AD-A089 422 MAY 80 J S KULPINSKI, T SIMONSEN, L CARROZZA RADC-TR-80-49 F30602-78-C-0195 UNCLASSIFIED NL

The circuit is used to measure line and load regulation on the LM117 and LM137 regulators. For the LM117 regulator the output voltage varies from 1.2 volts to 1.3 volts. With the voltage standard set to - 1.056 volts, the op amp output is

$$v_M = 4.42 v_0 - 1.056 (4.42)$$

and for 1.2 $v \le v_0 \le 1.3 v$

.63 6 volts
$$\leq$$
 $V_{M} \leq$ 1.078 volts

When two successive measurements are made, the two measured values are

$$v_{\rm M}' = 4.42 \, v_{\rm o}' - 4.66752$$

$$V_{M}^{\prime\prime} = 4.42 V_{O}^{\prime\prime} - 4.66752$$

These measurements are subtracted to determine the differential voltage,

$$v_{M}' - v_{M}'' = 4.42 (v_{O}' - v_{O}'')$$

and the voltage regulation is determined by the expression

$$\Delta V_0 = V_M' - V_M''$$

Output voltage measurements are made by using a resistive voltage divider network. The network divides the voltage so that for an output voltage range 1.2 V \leq V₀ \leqslant 1.3 V, the measurement voltage range is .923 V \leq V_M \leq 1.0 V. This permits measurements to be made at the top end of the 1 volt range rather than at the bottom of the 10 volt range. An alternate test circuit for these measurements is discussed in Section 3.5.

3.3.1.2.2 I_{ADJ} and I_{SCD} Current Tests (Line & Load)

I_{ADJUST} currents of the LM117 & LM137 are measured while performing line and load regulation tests by using a current-to-voltage amplifier. The main reasons the S-3263 current measuring capability is not used is as follows:

- 1) inadequate accuracy & resolution for ΔI_{ADJ} measurements
- 2) reduces the chance of damage to test system if gross failure of device under test occurred.

The current-to-voltage amplifier uses an LF155 op amp which is selected because of its low input bias current and because this minimizes errors. The gain is selected for the best DVM measurement range. The output of the amplifier is then coupled to an external voltmeter under IEEE bus control. The relationship of the measured voltage to the current is

$$I_{ADJ} = \frac{V_{M}}{R_{f}}$$

The amplifier is also used to measure the I_{SCD} current for the 4-terminal regulators. Relays are used to control the currents applied to the op amp summing point.

3.3.1.2.3 IO Test and ICONTROL Test

The current-to-voltage amplifier design includes a mode of operation that allows forcing of its summing point to a specified voltage value. When the quiescent current (I_Q) is to be measured for the LM117, the summing point is forced to 1.4 volts and is connected to the regulator output terminal. The current that flows out of the regulator under these conditions is the quiescent current. The measured amplifier output voltage and the quiescent current have the relationship

$$I_Q = \frac{(v_M - v_F)}{R_f}$$

For the LM137 the forced voltage is - 1.4 volts and the circuit operation is as defined above. \cdot

The measurement of the I_{CONTROL} current for the 4-terminal regulators is similar. The control pin is connected to the summing point and is forced to the proper voltage by setting the amplifier non-inverting input voltage (5.0 volts for the positive regulators and -2.23 volts for the negative regulators). The measured amplifier output voltage and the control current have the relationship

$$I_{CONT\,ROL} = \frac{(V_{M} - V_{F})}{R_{f}}$$

In addition to steering the proper currents to the summing point, relays are used to change the current-to-voltage gain for the control current measurement.

3.3.1.2.4 IOS, IPEAK & VOUT Recovery Tests

Short circuit (I_{OS}) and peak output current (I_{PEAK}) tests are performed by programming the load circuit power Darlington network into a second mode via relay control & S-3263 system. This mode of operation forces the output voltage of the regulator for a given time into short circuit ($V_{OUT} = \emptyset$ V) on I_{PEAK} current conditions (forces to predetermined regulator output voltage). The resultant currents are measured through a l ohm sensing resistor in series with the Darlington circuit via the S-3263 measurement subsystem.

The $V_{\rm OUT}$ (recovery) test is measured by first removing the regulator from the forced output condition and then allowing the output voltage to recover into a resistor, capacitor load after a given time. This test was added to determine if the regulator is capable of re-starting itself after short circuit conditions and provides important application information to the user of the regulators.

3.3.1.2.5 VSTART Tests

The start-up circuit consists of an input Darlington circuit which provides the necessary fast turn-on characteristics as well as a programmed input voltage to the regulator's input. The start-up circuits shown in Figures 3.7 & 3.8 measure the ability of the regulator to respond to extreme combinations of input voltage, and load currents by measuring the output voltage after a predetermined time. The load resistance during testing is shunted by a 20 ufd capacitor to simulate total distributed by-pass capacitors found in many system applications.

Although, I_{OS} , I_{P^*EAK} & V_{OUT} (recovery) tests are listed separately they are, in fact, combined as part of the V_{START} tests and provide a very subjective set of conditions to the regulator. The order in which the tests are performed is shown in Figures 3.12 & 3.13 and is stated as follows:

- 1) Starting circuit applies input voltage to regulator.
- 2) I_{OS} or I_{PEAK} test forces the regulator output to the specified voltage value and
- 3) $V_{\mbox{OUT}}$ recovery test allows the regulator to recover into a load circuit.

3.3.1.3 Test Accuracies And Correlation

All of the adapter test circuit gains and scaling factors are determined by using a precision voltage standard and a precision voltmeter. The precise gain value is used in the software program to calculate the test results from the measured data. Aside from some initial circuit stability problems, the most basic problems encountered while developing the test circuits and programs dealt with the S-3263 machine measurement accuracy. The S-3263 could not achieve, by itself, the accuracy or resolution necessary to meet the desired 10:1 test accuracy required for good test measurement systems. Essentially, the accuracy problems encountered during the measurement of the test parameters are overcome by increasing the gain of the signal to be measured and by level shifting the signal value to allow use of the most accurate portion of the most accurate measurement range.

Without the use of the current-to-voltage amplifier, the test system resolution on any current range would be sufficiently bad to render the $\Delta \, I_{ADJ}$ measurements meaningless. The current-to-voltage amplifier has a gain of 2000 V/A for all I_{ADJ} , I_{SCD} AND I_Q measurements and its gain is 33200 V/A for the $I_{CONTROL}$ current measurement. The desired measurement accuracy for measuring V_{out} was readily achieved by scaling the signal voltage to a more accurate part of the voltmeter range. However, because of resoltuion these measured values were too inaccurate to be used to calculate line and load regulation. The test circuit described in section 3.3.1.2.1 provides a gain of approximately 4.42 over the direct output voltage measurement and gives sufficient accuracy.

The results of the test accuracies achieved during characterization are shown in Table 3.11. There are few parameters where the S-3260 tests failed to meet the desired 10:1 test accuracy.....

As can be seen from Table 3.11, the basic S-3263 measurement accuracy would have failed to meet the 10:1 test accuracy. However with the additional circuitry incorporated into the S-3263 test adapter, the desired results were achieved.

A plot of the measured voltage vs percent error voltage on the S-3263 shows the basic capability of each range. Factored into these curves are the following:

- 1) percent of range
- 2) offset voltage
- 3) resolution

Another concern in selecting measurement ranges is the time required to sample and the time for the measurement system to settle out. An example of the types of problems encountered while selecting S-3263 ranges is as follows:

- 1) 100 mV range: best resoltion, worst accuracy, worst settling time
- 2) 1 & 10 volt range: best accuract, sest settling time
 However in making delta measurements of Vout,
 the resolution can be a significant error
 term, and a dominating factor when selecting
 ranges.

over all, the S-3263 still has one of the best sampling rates (200 samples/sec) which exceeds an external IEEE DBM by at least an order of magnitude. However, it is still necessary to consult the S-3263 measurement accuracy table before developing S-3263 test capability. Figures 3.14 through 3.18 show the basic test system accuracies for each voltage range.

The initial attempts to correlate data on the S-3263 test system to bench data, brought to light the system inadequacies in making measurements discussed above. The predominate errors were the gross instabilities of the delta measurements as a result of the machine resolution. At this time, the machine accuracies were checked for each measurement and the need for special test circuits was determined. With the addition of the new circuits to the adapter, correlation was checked and found to be well within the 20% requirement for correlation (ie 10% measurement error for each test set up).

Bench measurements were made using the test adapter as a carrier for the DUT. The adapter was checked to determine that it was capable of forcing the proper voltages and currents by programming the test circuits. Currents were checked by inserting an ammeter in series with current to be measured. Voltage measurements were then converted to calculated current values and were compared with the measured values. Absolute voltage measurements were taken at the DUT pins and were compared with the measurements at the sense line outputs and finally load regulation measurements were checked on an oscilloscope using a differential input pre-amplifier capable of measuring 10 mV/cm while the load current was changed the specified amount. The actual output voltage measurements at the DUT were then compared to the differential amplifier output measurements.

3.3.2 Dench Tests

Dynamic tests for the voltage regulators include a) ripple rejection, b) line transient response, c) load transient response and d) output noise. These tests were run on the LM117 and LM137 adjustable voltage regulators. No dynamic tests were run on the 78MG, 78G, 79M9 and 79G because of their similarity to the 7800 and 7900 voltage regulator families which were characterized on a previous contract.

Bench test circuit schematics are shown in Figures 3.19 thru 3.26. The noise test circuit schematics are shown in Figures 3.19 & 3.20. The test is performed using an oscilloscope with a differential preamplifier that has bandwidth control. The bandwidth was set to have a pass band from 10 Hz to 10 kHz and the peak-to-peak measurement of the noise was made. The ripple rejection test circuit schematics are shown in Figures 3.21 & 3.22. The test was performed using the above oscilloscope. The bandwidth was adjusted to reduce the high frequency noise without affecting the 2400 Hz ripple frequency. The 2400 Hz ripple at the regulator was measured on the oscilloscope as a peak-to-peak voltage. Line transient response and load transient response test circuit schematics are shown in Figures 3.23 thru 3.26. The peak measurements were made on a high frequency oscilloscope.

3.4 Test Results and Evaluation of Data

3.4.1 LMl17H Adjustable Positive Voltage Regulator

Tabulation of static test data taken on the S-3263 Automatic Tester for the LM117H Adjustable Positive Voltage Regulators is shown in Tables 3.12 thru 3.14. Because of the small sample of ten devices statistical analysis of the data was not performed. All of the devices save one met all of the parameter tolerances recommended by JC41 Sub-Committee on voltage regulators. The one device, serial number 4, failed load regulation. The specification for this parameter is 3.5 mV. The measured value was -4.75 mV. Analysis of this failure was done by measuring the device parameter in a bench set up using an oscilloscope. Pictures of the measurements were taken at the case. on the output lead 1/8 inch below the case, and on the output lead 3/8 inch below the case and are shown in Figures 3.27 thru 3.29, respectively. The load regulation measurements at these points were approximately 1 mV, 4.5 mV and 9 mV, respectively. As a result of contact with the vendor, on this and other similar failures reported herein, it was learned that the leads on the TO-5 type cases are made of Kovar. The resistivity of Kovar can be as much as 28 times that of copper (see reference 5, section 3.6). This high resistivity is the reason for the high load regulation measurements. The results and recommendations associated with this problem are discussed in Section 3.5.2.

Two units, serial numbers 5 and 6, tailed thermal regulation at -55 C. Since this measurement is not recommended at either -55 C or 125 C, these devices were not considered failures. However, these two units have been sent to the vendor for their measurement and analysis.

Tabulation of dynamic test data taken in a bench test set up for the LM17H Adjustable Positive Voltage Regulators is shown in Table 3.15. The tests were performed at 25°C and are of a) ripple rejection, b) output voltage noise, c) line transient response and d) load transient response. All of the bench measurements made on these devices were stable and showed reasonable sate margin for the recommended tolerances. Oscillographs of the Line and Lead Transient Responses are shown in Figures 3.30 and 3.31.

3.4.2 LM117K Adjustable Positive Voltage Regulators

Tabulation of static test data taken on the S-3263 Automatic Tester for nine LM117K adjustable positive voltage regulators is shown in Tables 3.16 thru 3.18. All of the devices met the tolerances recommended by the JC41 Subcommittee on Voltage Regulators.

Tabulation of dynamic test data taken in a bench test set up is shown in Table 3.19. All of the devices met the tolerances recommended by the JC-41 Subcommittee on Voltage Regulators. Oscillographs of the line and load transient responses are shown in Figures 3.32 and 3.33.

3.4.3 LM137H Adjustable Negative Voltage Regulators

Tabulation of static test data taken on the S-3263 Automatic Tester for ten LM137H Adjustable Negative Voltage Regulators is shown in Tables 3.20 thru 3.22. All of the devices failed load regulation for current changes from 5-to-500 mA. The vendor was contacted on this matter and confirmed the problem. The vendor has issued a letter on this problem and recommends that the current changes be reduced to 5-to-200 mA. The devices met all other parameter tolerances recommended by the JC-41 Subcommittee on Voltage Regulators.

Tabulation of dynamic test data taken in a bench test set up is shown in Tables 3.23. The devices met all of the parameter tolerances recommended by the JC-41 Subcommittee. Oscillographs of the line and load transient responses are shown in Figures 3.34 and 3.35.

3.4.4 LM137K Adjustable Negative Voltage Regulators

Tabulation of static test data taken on the S-3263 Automatic Tester for eight LM137K Adjustable Negative Voltage Regulators is shown in Tables 3.24 thru 3.26. The devices met all of the parameter tolerances recommended by the JC-41 Subcommittee.

Tabulation of dynamic test data taken in a bench test setup is shown in Table 3.27. The devices met all of the recommended parameter tolerances. Oscillographs of the line and load transient response are shown in Figures 3.36 and 3.37.

3.4.5 Comparison of Test Data on 3-terminal Devices

The average values of the measurements of the 3-terminal adjustable voltage regulators is shown in Tables 3.28, 3.29 & 3.30 for temperatures of 25°C, - 55°C & 125°C, respectively.

3.4.6 Four-terminal Devices

Because of the similarity in the design of the 4-terminal adjustable regulators to their 3-terminal fixed voltage counterparts, a full characterization effort of these devices was not originally planned. Some one ampere negative adjustable regulators with date codes 7639 showed some anomalies in their electrical performance. Devices with more recent date codes have been requested from the vendor and data will be obtained on these parts for the next report.

3.5 Conclusions and Recommendations

3.5.1 Test Circuits

The large currents (> 1 Amp) required to test these and future voltage regulators cannot be supplied or controlled by most automatic test systems. The test circuits designed for testing these voltage regulators are capable of interfacing with external power supplies and forcing the DUT input voltage levels and output load current levels. The power Darlington transistors can readily carry and control the 5 amps needed for the short circuit current and start-up tests; however, future voltage regulators needing 2-3 times this current will require different Darlington transistors than those used for these characterization efforts. The op amps used in these test circuits have relay switches connected to their inputs that change their operating mode during the test. Because of these switches, special stabilizing circuits may be required for the op amps.

The low level input circuits can be controlled by any automatic test system capable of forcing voltages between + 15 volts and - 15 volts. Although the test technique for measuring line, load and thermal regulation was adequate for these characterization efforts, it required a DC voltage standard. A more complex circuit is shown in Figure 3.38 which may be more desirable for production testing when additional resolution is needed by the test system.

The regulator output is simultaneously applied to the input of the sample/hold amplifier and to one input line of the summing amplifier. Prior to a time $t=t_0$, the S/H amplifier is in the sample mode. At $t=t_0$, the S/H amplifier is switched to the hold mode. After settling, the output voltage of the summing amplifier is measured. This voltage is an error signal (E) and is nominally 0 volts. At $t=t_1$, the regulator is stimulated to a new line/load condition. At a predetermined time after this (ie .5 ms), the output voltage ($V_{\rm S}$) of the summing amplifier is measured. This measurement is proportional to the difference between the voltage regulator output at $t_1+.5$ ms and the voltage regulator output at t_0 . From these measurements we can calculate that the regulation is

$$\Delta V_R = \frac{V_s - E}{(R_f/R_i)}$$

3.5.2 Devices Under Test

The voltage regulators discussed in this section were tested on the S-3263 to determine their static electrical characteristics at 25°C, -55°C and 125°C. The devices were also tested in a bench type test setup to determine their dynamic (ie. transient AC) electrical characteristics at 25°C. The data shown in Tables 3.12 thru 3.27 indicates absence of data from some parts. These parts failed during test development as a result of improper voltages or polarity being applied to the regulators. None of the devices is known to have catastrophically failed in an operating test circuit.

The most significant parameter failure was the failure of load regulation for the LM137H voltage regulator. The vendor has confirmed these failures and suggests that load regulation, for $\rm V_{in}=-6.25~V$, be performed for 5 mA $\rm I_L \leq 200~mA$. OS agrees with this decision; however, since the part is a 500 mA voltage regulator, it should also have a load regulation test performed for 5 mA $\rm I_L \leq 500~mA$. OS also recommends that the limits shall be $\pm~20~mV$ at 25°C and $\pm~25~mV$ for $-55^{\circ}\rm C \leq T_A \leq 125^{\circ}\rm C$.

There is evidence in the published literature (reference 6, Section 3.5) that start-up and voltage recovery problems exist in some 3-terminal fixed voltage regulators. When the output of the regulator is shorted to ground under conditions of high input voltage, the safe area protection circuit turns on and may force the regulator output current to zero. Under these conditions, the safe area protection circuit maintains a zero current condition even after the short is removed. Consequently, the voltage regulator may not recover from a short circuit condition until the input voltage is removed and then reapplied. The timing sequence (shown in Figures 3.12 and 3.13) has been devised by OS to provide a rapid start-up condition into a maximum load resistance to insure start up with a voltage

step function, from 0 to V_{in} , at the DUT input, b) a short circuit condition at the output to measure the current limit and c) voltage recovery check to insure that the device will recover under a maximum resistive load co dition when the short circuit is removed. This test has been recommended by 0S to provide functional assurance of the device's start-up capability under adverse system conditions. The test conditions and parameter tolerances recommended by 0S and the JC-41 Subcommittee on Voltage Regulators are shown in Tables 3.29 thru 3.36.

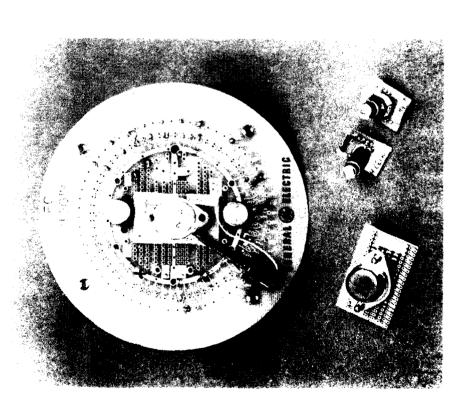
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- 3. RADC-TR-78-22 Final Technical Report: J. S. Kulpinski et al, General Electric Company 1978. (A052357)
- 4. RADC-TR-78-275 Final Technical Report: J. S. Kulpinski et al, General Electric Company, 1979. (A065997)
- 5. Reference Data for Radio Engineers; H. P. Westman, editor, International Telephone and Telegraph Corporation, 1957.
- 6. Designer's Guide To: IC voltage regulators: Robert C. Dobkin, National Semiconductor Corp., EDN August 20, 1979 and September 5, 1979.

III-21

(Bottom view)

Figure 3.8. Voltage Regulator Test Adapter.



(Top view)
Figure 3.7. Voltage Regulator Test Adapter.

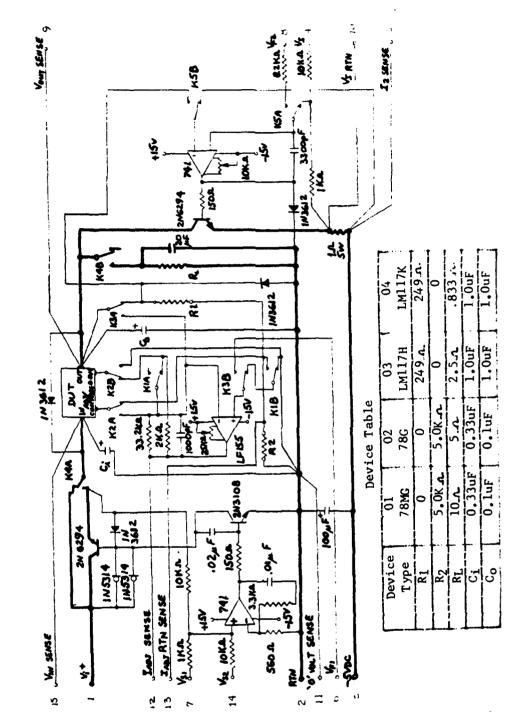
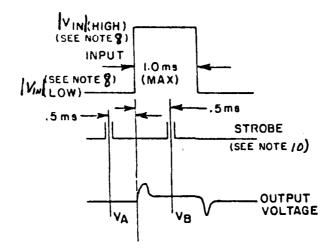


Figure 3.9. Positive voltage regulator test circuit for static tests.

LINE REGULATION WAVEFORMS



LOAD REGULATION WAVEFORMS

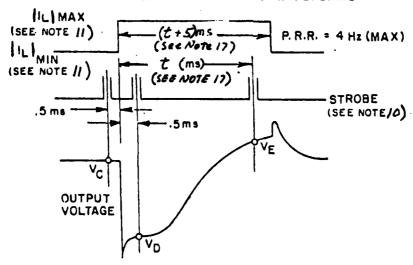


Figure 3.9. Positive voltage regulator test circuit for static tests (cont'd).

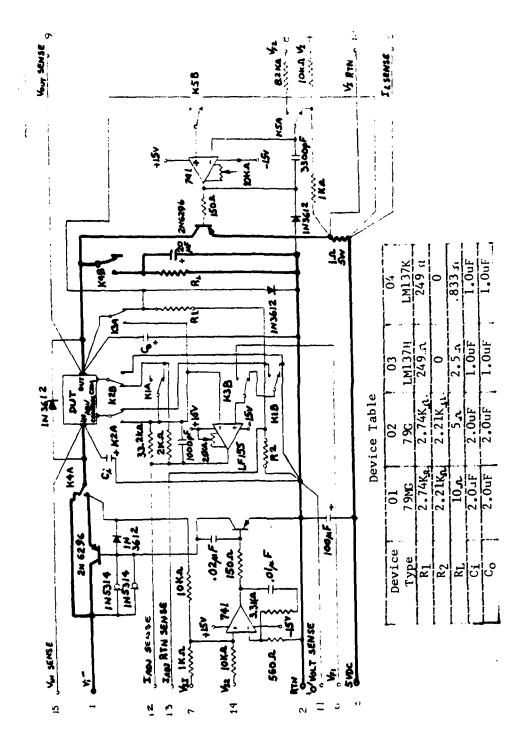
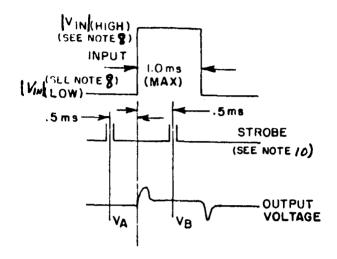


Figure 3.10. Negative voltage regulator test circuit for static tests.

LINE REGULATION WAVEFORMS



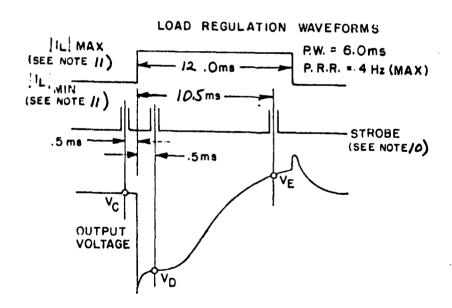


Figure 3.10. Negative voltage regulator test circuit for static tests (cont'd).

REGULATOR VO
OUTPUT
VOLTAGE
IOKA
10KA
44.2KA
44.2KA
7+15V

STANDARD
IOKA
10KA

Figure 3.11. Level shift circuit and amplifier for $v_{RLINE},\ v_{RLOAD}\ ^{\&}\ v_{RTH}$ tests.

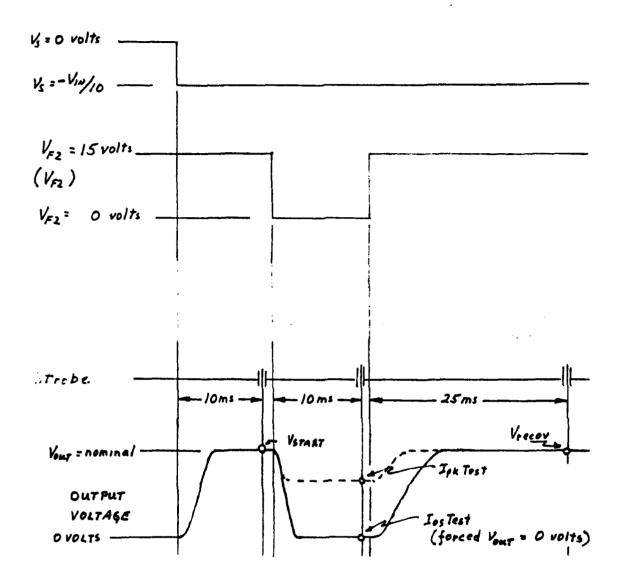


Figure 3.12. Positive voltage regulator timing sequence for $\rm V_{START}$, $\rm I_{OS}~\&~V_{OUT}$ RECOV.

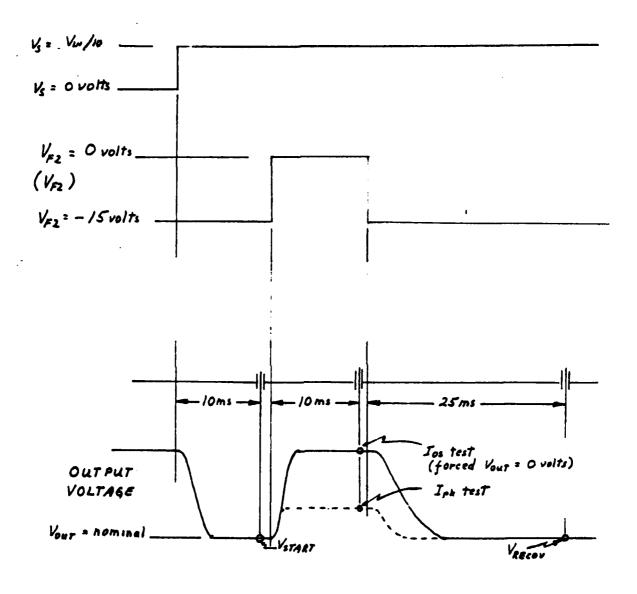


Figure 3.13. Negative voltage regulator timing sequence for $\rm V_{START}$, $\rm I_{OS}$ & $\rm V_{OUT}$ RECOV.

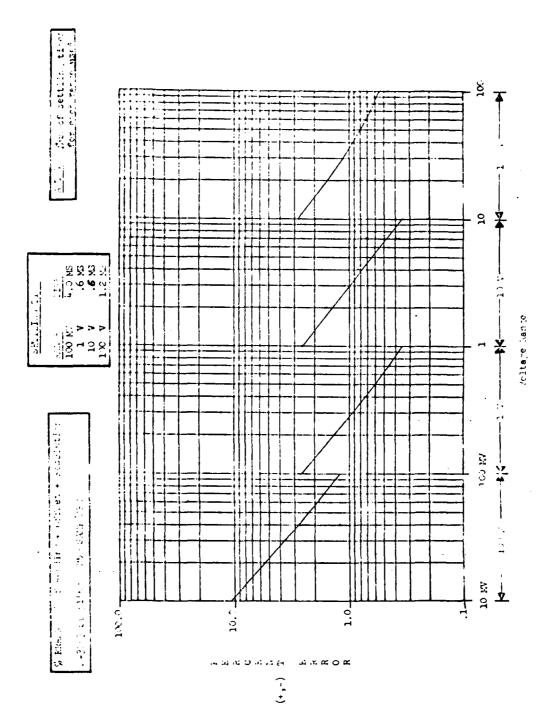
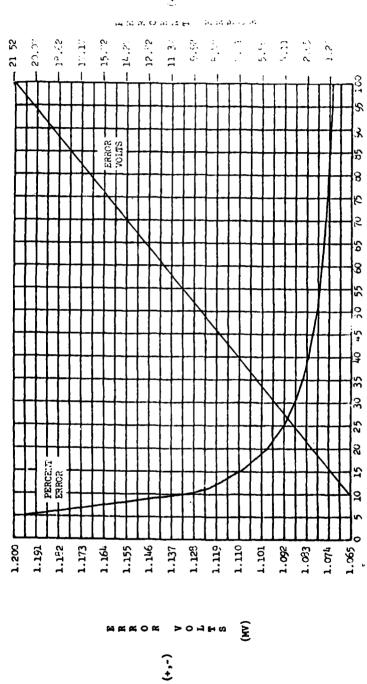


Figure 3.14. S-3263 Test System Differential Voltage Accuracy.





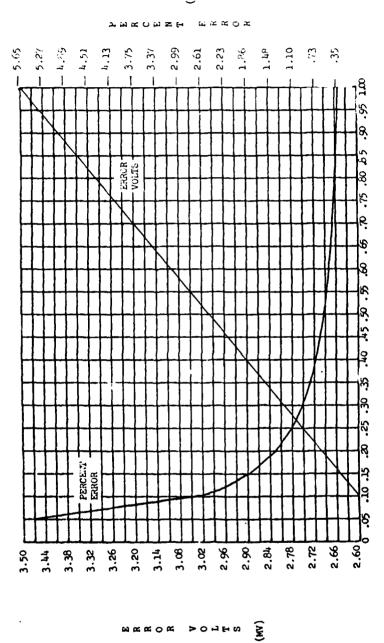
100 NV Range = :(0.15% of Reading + 1 NV + .05% of Range

Figure 3.15. S-3263 Test System Differential Voltage Accuracy

100 MV Range

III-31





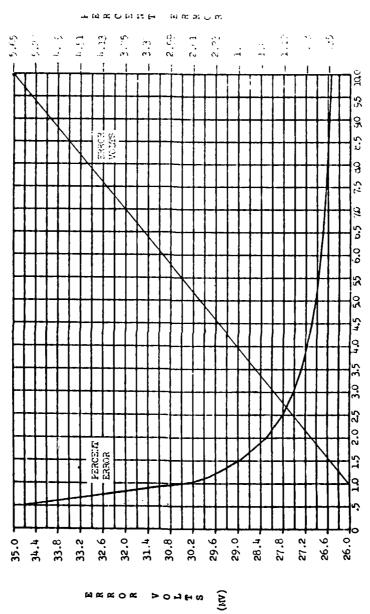
1 Volt Range = $\pm (0.1\% \text{ of Reading} + 2.3V + .05\% \text{ of Range})$

1 Volt Range Figure 3.16, S-3263 Test System Differential Voltage Accuracy

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(-, ÷)





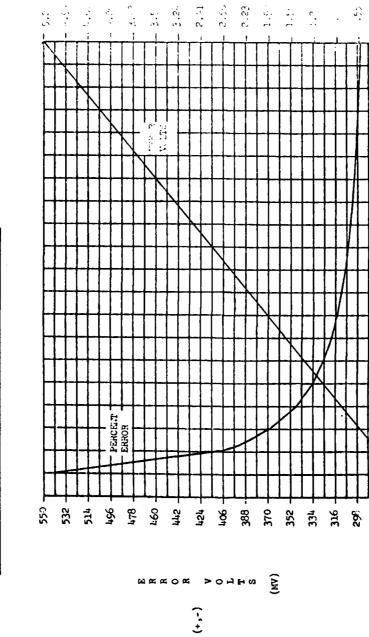
10 Volt Range = ±(0.1% of Reading + 20 MV +.05% of Range)

Figure 3.17. S-3263 Test System Differential Voltage Accuracy

10 Volt Range

(÷,÷)





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Figure 3.18. S-3263 Test System Differential Voltage Accuracy

100 V Range

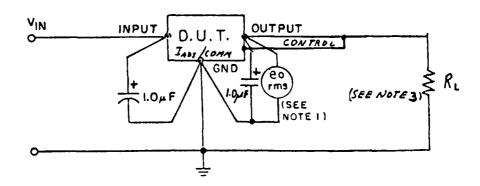
95 100

88 88

75 80

& &

比

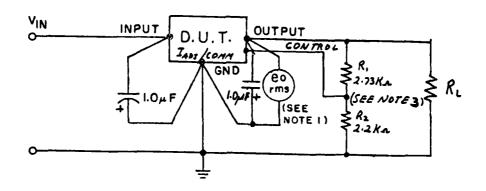


Device Table						
Device	01	02	03	04		
Type	78 MG	78 G	LM117H	LM117K		
VIN	10 V	10 V	6.25 V	6.25 V		
$R_{ m L}$	_م_100	ـمـ 50	25_مـ	ـمـ 12.5		

 $R_{\overline{L}}$ shall be type REF 70 or equivalent.

- The meter for measuring e_{Orms} shall have a minimum bandwidth from 10 Hz to 10 kHz and shall measure true rms voltages.
- 2. $N_0 = e_0 \text{ rms.}$
- 3. The control pin connection is required for device types 01 and 02 only.

Figure 3.19. Noise test circuit for positive voltage regulators.

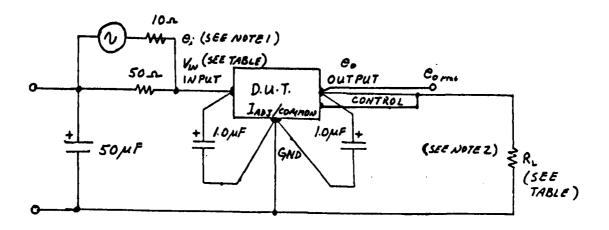


Device Table						
Device	04					
Туре	79 MG	79 G	LM137H	LM137G		
v _{IN}	-10 V	-10 v	-6.25V	-6.25 V		
RL	100مـ	50.1	ـمـ 25	12.5 _n _		

 R_{L} shall be type RET 70 or equivalent.

- 1. The meter for measuring e_{Orms} shall have a minimum bandwidth from 10 Hz to 10 kHz and shall measure true rms voltages.
- 2. $N_0 = e_0 \text{ rms}$.
- 3. The control pin connections and resistors (R_1 and R_2) are required for device types 01 and 02 only.

Figure 3.20. Noise test circuit for negative voltage regulators.

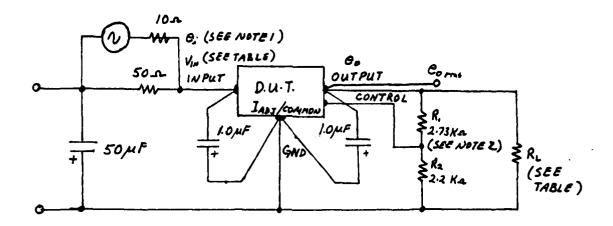


Device Table						
Device	01	02	03	04		
Type 78 MG		78 G	LM117H	LM117K		
V _{IN} 10 V		10 V	6.25 V	6.25 V		
R_{L}	40.2	14.3م	ـمــ10	2.5_1		

The input 50.1 resistor and \mathbf{R}_L shall be type RER 70 or equivalent.

- 1. $e_i = 1 \text{ V}_{rms}$ @ f = 2400 Hz (measured at the input terminals of the DUT) ripple rejection = 2- $\log \frac{e_i^{rms}}{e_o^{rms}}$
- 2. The control pin connection is required for device types 01 and 02 only.

Figure 3.21. Ripple rejection test circuit for positive voltage regulators.

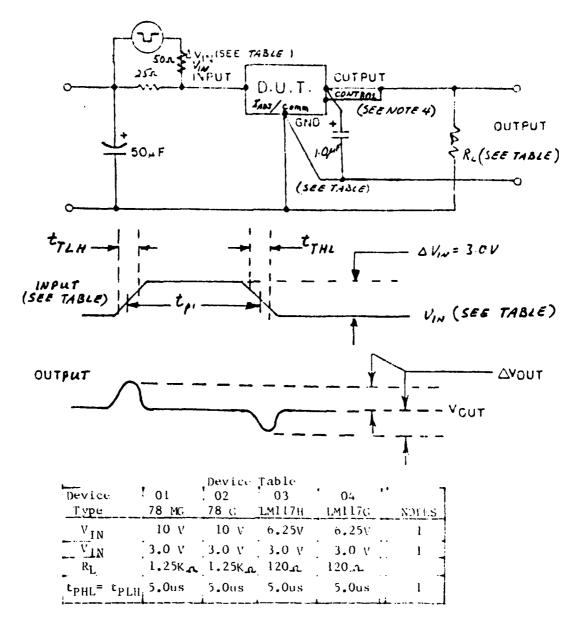


Device Table						
Device	03	04				
Type	79 MG	79 G	LM137H	LM137K		
·						
VIN	-10 V	-10 V	-6.25 V	-6.25 V		
R _L	40.2م	14.3_م	يم_10	2.5_2		

The input 50 $\mbox{\ensuremath{\Lambda}}$ resistor and $R_{\rm L}$ shall be type RER 70 or equivalent.

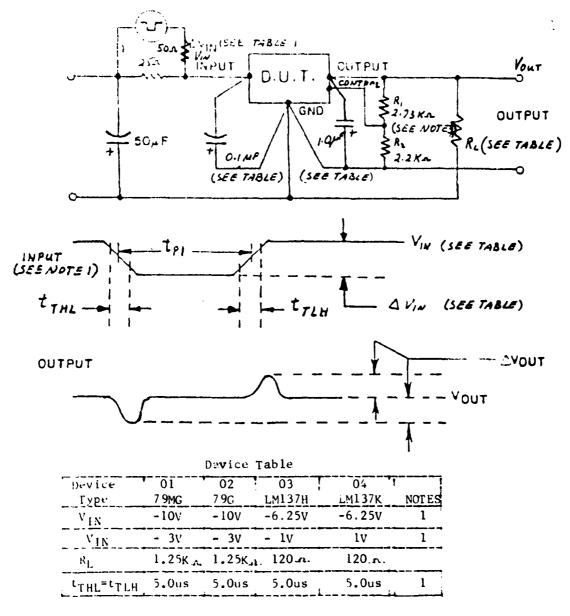
- 1. $e_i = 1 \text{ V}_{rms}$ @ f = 2400 Hz (measured at the input terminals of the DUT) ripple rejection = 20 log $\frac{e_{irms}}{e_{orms}}$
- 2. The control pin connection and resistors (R_1 and R_2) are required for device types 01 and 02 only.

Figure 3.22. Ripple rejection test circuit for negative voltage regulators.



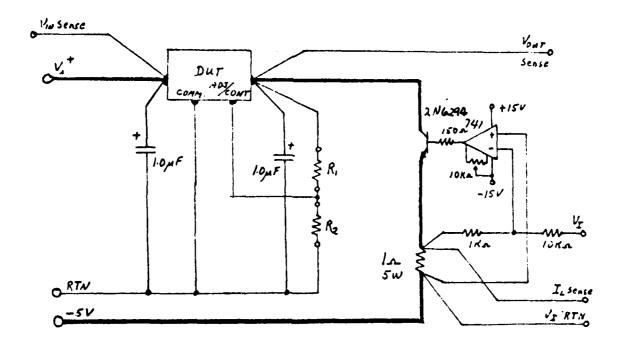
- 1. Measured at device input.
- 2. Pulse width $t_{p1} = 25$ us; duty cycle 3. (maximum)
- 3. Oscilloscope bandwidth = 5 MHz to 15 MHz.
- 4. The control pin connection is required for device types 01 and 02.

Figure 3.23. Line transient response test circuit for positive voltage regulators.



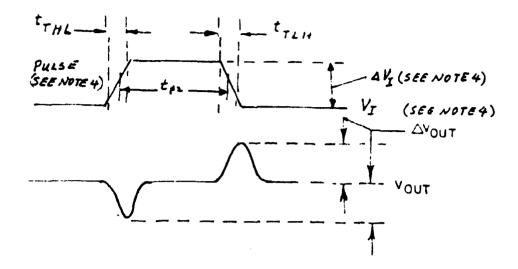
- 1. Measured at device input.
- 2. Pulse width $t_{pl} = 25$ us; duty cycle = 3 / (maximum)
- 3. ()scilloscope bandwidth = 5 MHz to 15 MHz.
- 4. The control pin connection and resistors (R_1 and R_2) are required for device types 01 and 02.

igure 3.24. Line transient response test circuit for negative voltage regulators.

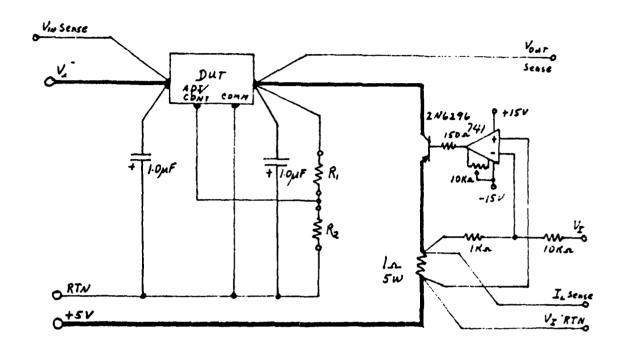


Device Table						
	Device	01	02	03	04	
	Type	78MG	<u> 7</u> 80	1.M117H	1,M117.G	
	RL	0	0	249 A.	249 7.	
	R2	5.0K.	3.0K a.	0	0	
	11,	-50mA	-100mA	- 50m.\	-100m\	
	ΙL	-200mA	-400mA	-200nA	400m\	
		-0.49V	-0,99\	-0.45	-0.951	
	<u> </u>	-2.0V	-4.0V	2.0V	-4.0V	

Figure 3.25. Load transient response test circuit for positive voltage regulators.

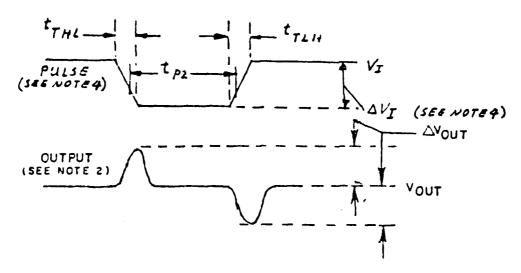


- 1. Heavy current paths (177 1.0A) are indicated by bold lines.
- 2. Solvin connections must be used for all output current and voltage measurements.
- 3. Operante stabilization networks may vary with test adapter construction. Alternate drive circuits for the 2N6294 may be used to develop the proper load current and input voltage pulses.
- 4. The pulse generator for the pulse load circuit shall have the following characteristics. (see device Table III)
 - a. coltage level $(C_1) = -10 (I_L Vo/(R_1 + R_2))$ volts
 - b. Pulse width (tp2) = 25 u sec.
 - c. Duty cycle = 3° (maximum)
 - d. $t_{THL} = t_{TLH} = 1.0$ used for device types 01 and 02
 - c till = till = 5.0 usec for device types 03 and 04
 - Difference voltage level $(\triangle V_I) = 10$ (I_I) volts
- 5. i. $25 \text{ V}_{\text{out}} = 500 \text{ mV}$ maximum for device type 01
 - b. 2. Vout = 1000 mV maximum for device type 02
 - c. $C_{\rm e}V_{\rm out}$ = 120 mV maximum for devices type 03 and 04 (fhese values guarantee the specified limits for load transient response.)
- 5. Oscilloscope minimum bandwidth shall be 9 MHz to 15 MHz.
- residence 3.2% road transfent response test circuit for positive voltage regulators (cont'd.).



	Device Table					
1	Device	01	02	03	04	
l	Type	7 9MG	7 %	LM137H	LM137K	
	R1	2.21K ₃	2.21K A.	249	249 n	
	R ₂	2.74Kr	2.74K s.	0	ō	
ſ	ī _L	50 nA	100m\	50m4	100 nA	
	l	200mA	400m.\	200 n∧	400m.\	
1	Vį	0.491	0.99\'	0.450	0.95\	
J	VΙ	2.0V	4.00	2.0\	4.01	

Figure 3.26 Load transient response test circuit for negative velta, e regulators.



- 1. Heavy current path (122 1.0A) are indicated by bold lines.
- 2. Relvin connections must be used for all output current and voltage measurements.
- 3. Op amp stabilization networks may vary with test adapter construction. Alternate drive circuits for the 2N6296 may be used to develop the proper load current and input voltage pulses.
- 4. The pulse generator for the pulse load circuit shall have the following characteristics. (see device table)
 - a. Voltage level $(V_1) = 10 (I_L + Vo/(R_1 + R_2))$ volts
 - b. Pulse width $(t_{p2}) = 25$ u sec c. Duty cycle = 3? (maximum)

 - d. t_{THL} = t_{TLH} = 1.0 u sec for device types 01 and 02 c. t_{THL} = t_{TLH} = 5.0 u sec for device types 03 and 04

 - Difference voltage level ($\triangle V_I$) = 10 (I_L) volts
- 5. a. $v_{\rm out}$ = 500 mV maximum for device type 01 b. $v_{\rm out}$ = 1000 mV maximum for device type 02

 - $c = 7.7V_{\rm GHT}$ = 60 mV maximum for devices type 03 and 04 (These values guarantee the specified limits for load transient response.)
- 6. Oscilloscope minimum bandwidth shall be 9 MHz to 15 MHz.
- in re 3.25. fead transient response test circuit for negative voltage regulators (cont'd).

LMITTH Load Regulation



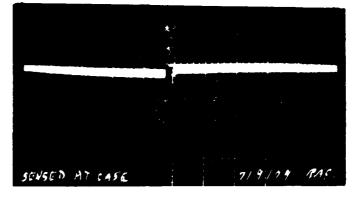
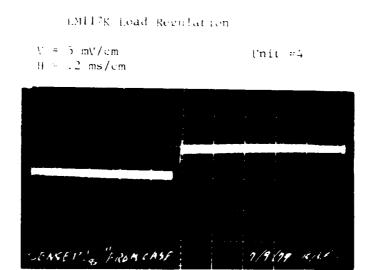
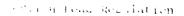
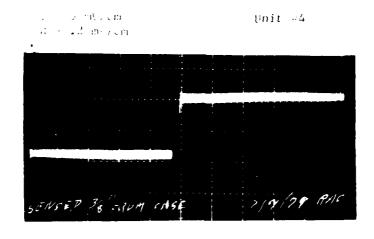


Figure 3 27. Oscillograph of Lillie Ladice state rope latter cases:



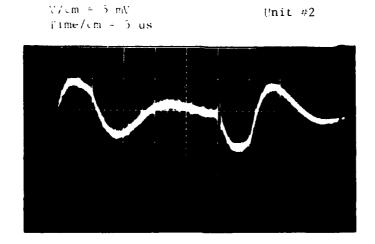
of the 3/28 (Scillograp of 1911) load regulation measurem 1755 will case



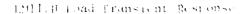


e 3.2%. \sim . However, or MMILH load regulation measured 3/8" below 105%.

LMI17H Line Transient Response



1 (4.3). Schiller at MILB line transient response test.



v/cm = .02 (init :10) Time/cm = 5 us

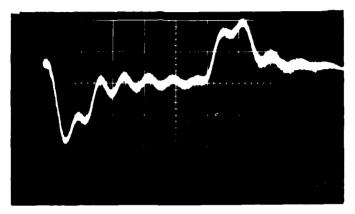


Figure 3.31. Oscillograph of AMILA load transient response test.

LM117K Line Fransient Response

v/cm = 5 mV t'nit = 2Time/cm = 5 us

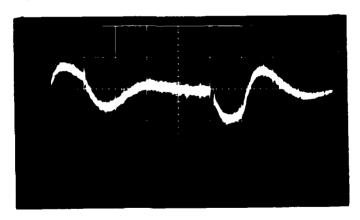
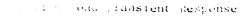
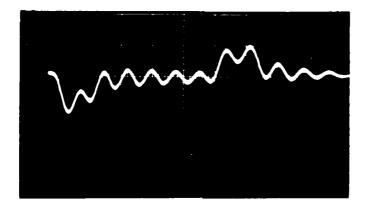


Figure 3.32. Oscillograph of CMID line transfect response test.



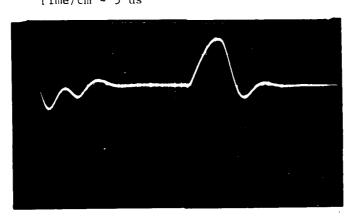
 $\begin{array}{ccc} \mathfrak{m} & \mathfrak{g}(0) & \text{ (init } \# 1) \\ \operatorname{the/sm} & \times \mathbf{us} & \end{array}$



increase. 33. escitionrap of 0.911% load transient response test.

LM137H Line Transient Response

V/cm = .020 Unit #1 [ime/cm = 5 us



There 3.34. Oscillorraph of LM137H line transient response test.



\forall / cm = .01
\forall \forall \forall cm = .05

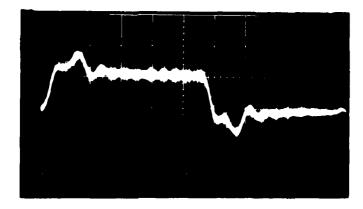


Figure 3.35. Oscillograph of CM1378 load transfent response test.

EM137K Line transient Response

V/cm = .020 Time/cm = 5 us

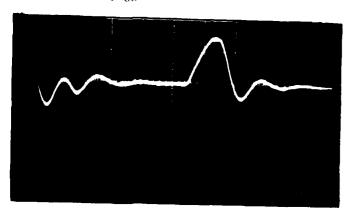
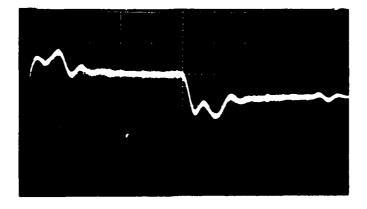


Figure 3.36. Oscillograph of LMB/K line transient response test.

IMIB/K Load Transfelt Response





there 3.3 describeraph for LN137K load transient response test.

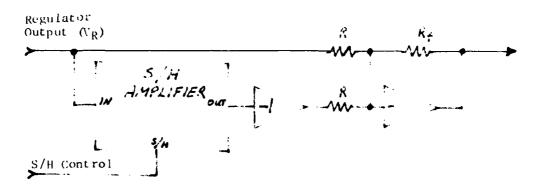


Figure 3.38. Alternate test circuit for v_{RLINE} , v_{RLINE} , $v_{RLOAD} \in v_{RIH}$ (ests

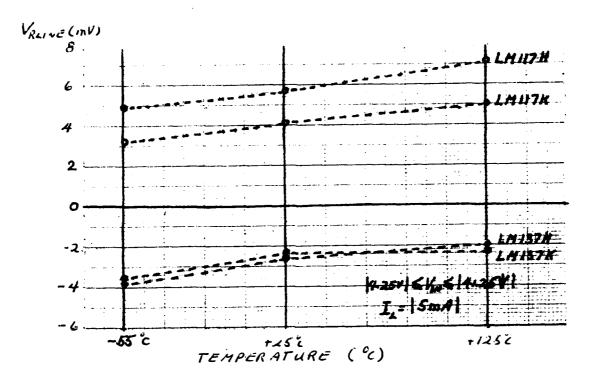


Figure 3.39. Average Line Regulation versus Temperature.

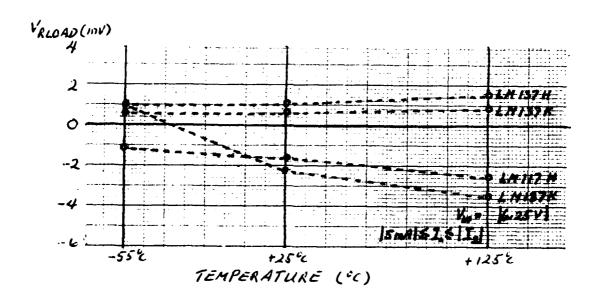


Figure 3.40. Average Load Regulation (#2) versus Temperature.

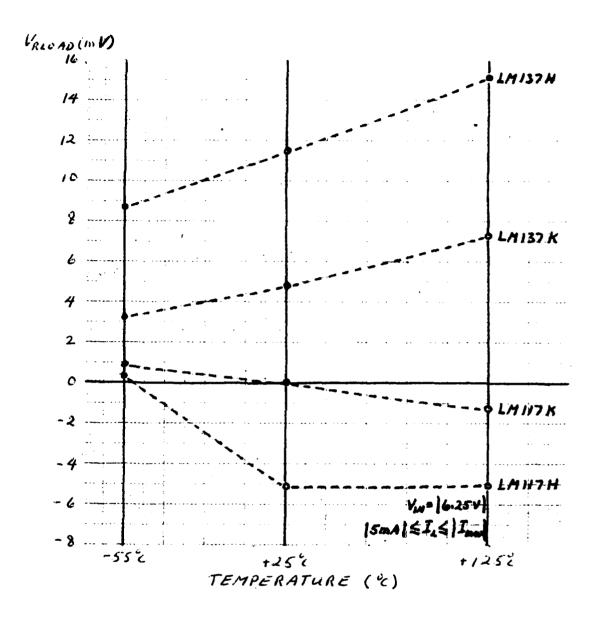


Figure 3.41. Average Load Regulation (#1) versus Temperature.

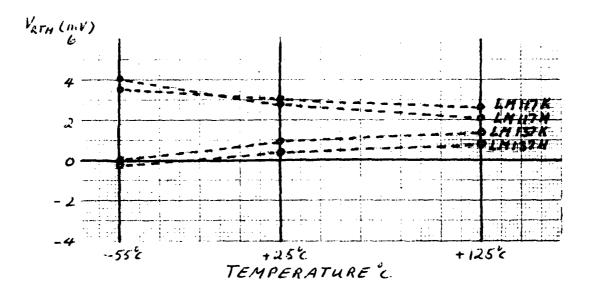


Figure 3.42. Average Thermal Regulation versus Temperature.

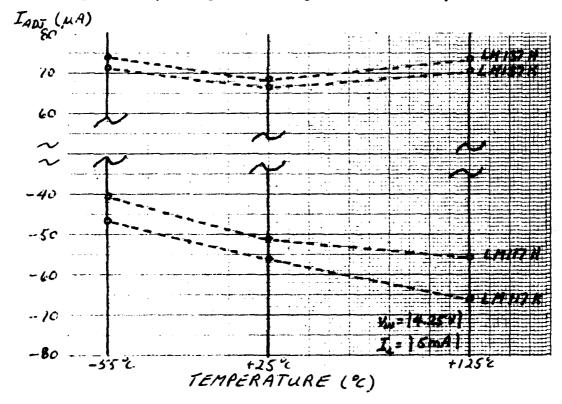


Figure 3.43. Average Adjustment Pin Current versus Temperature.

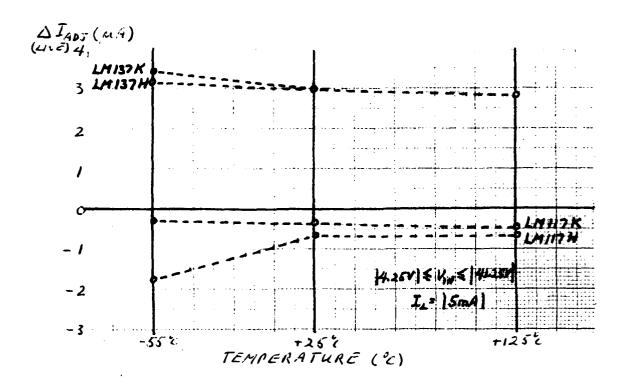


Figure 3.44. Average Change of $I_{\mbox{ADJ}}$ with Line Voltage versus Temperature.

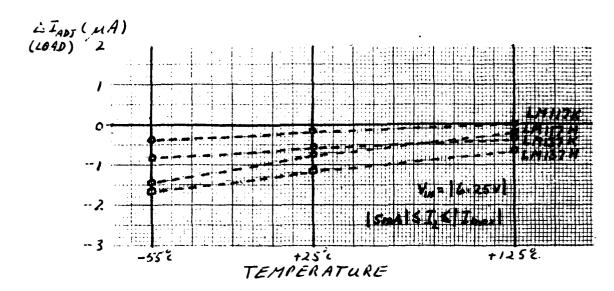


Figure 3.45. Average Change of $\mathbf{I}_{\mbox{ADJ}}$ with Load Current versus Temperature.

(x,y,y,y,z) , as the decrease for external and starteness to a frace of the contract of the x

Symbol	.es1		i je	Tied		Volta		Relays Energi zed		rement	•	Equation	u
	1 2000 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	I I	12105	/11) PINS 4-5	Pins	• :	8-2	İ	Pins Hi-Lo	[Value]	Ur.its		Š
1/0471 10472	38	-5 -500		-04	-	-	-	None	9-11	E, E2	V.	Vouts = E, Vouts = E2	Y
Cut 3		-500	20	4.99	-	-	-			E3 E4 E5		Vout 3 = E3 Vout 4 = E4 Vout 5 = E5	
10175 10175 121161	30 30	-50 -50	30	49 49					_ _	E		Valles E, E &	hiv'
ALINE	8	350 350	8	3.49 3.49	-	- -	- -			E8 E9		VRI, NE 2 = E8 - E9	•
ALCAD!	15 10	-5 -500	10	4.99		1 1	1 1 1			E10 E11		VRLOADI VRLOADI VRLOADI=E5-E6	
FRTH		500		4.99	_	-	-			EIZ	- -	VRTH = E12-	
Iscos I _{sco} 2		-5 -5		.04	-	-	-		12-13	E13 E14	. _	Isco = E13/2000 Isco = E14/2000	m/4 - -
AISED (LIVE) AIRE		-5 -500	10	.04 -4.99	_	-	<u>-</u>	\		E15	-	$ \begin{array}{ll} \Delta I_{SCD} = \underline{E_{IS}} - \underline{E_{I}}, \\ (LINE) & \underline{2000} \end{array} $ $ \Delta I_{SCD} = \underline{E_{IS}} - \underline{E_{IS}} $	- [-
Loss:	10		15	<u>-</u>	1 1	1.0 1.0	0	K4, K5	10-5 9-11	E17 E18	- -	(LOAD) 2000 IOSI E17 YOUT = E18	A
ICSI	25	-	30	-	-	2.5 2.5	0		10-5 9-11	Ezo		I = E19 Vour = E20	AV
Toss	30	-	40	-	_ _	3.5 3.5	0	į	10-5	E ₂₁ E ₂₂		I os = E21, Vour = E22	A
Vout (RECOVE Iph	.30	_	15		_	0.8			10-5	£23	- -	$I_{pk} = E_{23}.$	A
Vout PECCU ICONT!	8 .'C	-350	15	- 3.49	-	0.8	_	NY 25 KI, KZ	9-11	E24	-	Vour = E24 Icon = E25/33200	V MA
VITART		500	15	_	-	0.8		К4	9-11	F 26	1	Vout = £26	V*

Table 3.4. Test conditions for a-terminal adjustable positive voltage regulator (780).

Symbol	Test	t Litiens	App	lied 171)	Test	Volta -Lo]	yes	Sela Enel	 y s			remen Lines	Τ	Equation	11
	V.,.	I. (md)	Pins	Pins	Pins	Pins	8-2	†	9.22.	pin hi-	5	Value	druts		F 3
Vouti	8	-5	8	-9.97		-	=	No.	ne	9-1	1	E,	V .	Vouts = E, Vouts = E2	. ``
Vout 3	11	-5	20			-	-					E3		Vours = Es	
VOHT4		1000		7.99	-	-	_			1 1		E4		1047 4 = E4	
Vour 5		-5 -100	30	99	-	_						Es		Vours = Es Vours = Es	
VRLING		-100	8	99	_	-	-			-		En	 	VRLINES = E, - EL	77.7
ALINE	9	500	8 -	4.99	-	-	-				!	EB			
PRLINE	25	500		4.99		_	-					Eq		VRLINE 2 = 58 - E9	
VRLDAD		-5	-	.04	_	_	-					EIO			
RLOAD	10	1000	10	9.99	-	-	_					€,,		VALOADI EID-EII	
RELAD	_	_			L					<u> </u>		_	_	VRLOAD2 = E5 - E6	_
RTH	15	1000	15.	9.99	-	-	-			Ť		EIZ		VATH = E12"	
Iscos	10	-5	10.	.04		-		_		12-1	3	E13		Isco = 613/2000	11.
Isco 2		-5	36	.04		_	_					E14		Iscoz = E14/2000	
AISCD (LINE)	8	-5	8	04		-	-					E15		$\Delta I_{(L,NE)} = \underbrace{E_{/S} - E_{,\gamma}}_{2000}$	
Δ I sc p (LO4D)	10	1000	10.	9,99	1	1	-	7				EIL		$\frac{\Delta I_{SCD} = E_{I3} - E_{I6}}{(LOAD)} = \frac{2000}{2000}$	
Icss.	10	-	15	-	-	1.0	0		. K5			£17		Icu En	4
(RECON	10	-	15	_	-	1.0	0	A 15		9-1		E18	1 1	Vout = E18	
Iosz	52	-	30	_		2.5	0	•		10-3		Eig	}	Iosi Eig	7
VOUT (RECOL	25	_	30	-		2.5	0			9-1	′.	Ezo		Vout = E20	• •
Ioss	30	-	40	-		3.5	0			10-	1	Ezi		$I_{os_3} = E_{21}$	7
Vout (RECOV	30	-	40	-		3.5	0	•	Y	9-1	1	E22		Vcur = = = 22	•
IPK	8	-	15	_	_	0.8		3.7	. [10-	5	\mathcal{E}_{λ_3}		Ipk = E23.	••
VOUT RECOVE	8	- 1	15	-	-	0.8		.7.4	• (9-11	/	\mathcal{E}_{2i}		VOUT = E24	
ICENT	لــــــــــــــــــــــــــــــــــــــ	500	10	4.99	_	-		KI,	KZ	12-1	3	E25		Icon = E25/33200	دومأ
V _{START}	8	1000	15	-]	-	0.8	-]	К	4	9-1	/	E 26	•	Vout = E26	•

Natice 3.7. Lest conditions for D-terminal accessfable positive voltage regulator of MIL $n_{\rm p}$.

	T		14	1.1		1/14		I Salana			+	Equation	1
7,74.	Test	,	1		Г	Volta pins	1	Relays Energized	Measu	remer Lines	11	2 40 41 10 11	
,	ļ · ·		(Vo	,		1-20	1	1	pins		Jairs	•	1
	1017:	I.	1-2	PINS 4-5	6-11		8-2		Hi-Lo	1.4146			ĺ
Vours		1-5	4.25	.1	-	-	} <i>"</i>	None	9-11	E,	V	Vouri= E,	1/
Vourz	7.2	1500	4 23	4.95	1 -	-	-			Ez		Voutz= E2	
FOUT 3		\$-5	41.2	0.45	-	_	_			E ₄		Voury = E4	
Joury	7/	1-50	77.2	†	 _	 	-	<u> </u>	 -	 	├		V
VRLIVE	-					<u> -</u>	_	 	- -	-	- -	VRLINE = E1-E3	mv
VRLOAD	N .	-5	6.25	•	-	-	-	1 1		Es		ري جي جي ال	} .
1 Rio 4D		500	625	4.95	1 -	-	-	[]		Eb	1	VRLOADS= Es- Es	
VRLOAD				_	<u> </u>	<u> -</u>	_	<u> </u>	 	-	┡ ╽	VRLOADE E3- E4	┝╷⊣
PETH	14.6	750	14.6	-7.45	-	-		+	1	E,	+	VRTH De Ex	•
I_{ADJ}	4.25	-5	4.25	0	-	-	_	K2	12-13	E	mV	IADS: E8/2000	MA
Ind	4/2	-5	4/25	0	_	-	-			Eg		IADJ = E9/2000	
ALAN	-	_	-	_	_	-	_			_		A IAW = E8-E0 LINE 2000	
(LINE)			ļ		ļ	ļ	ļ		├		- - -	21NE 2000	- ; -
(LCAB)	6.25	-5	625				_		,	Eio		1405 = E10-E11	
LOAD (LOAD)	625	500	6.25	4.95	_		_	Y	1	\mathcal{E}_{II}	*	(LOAD) 2000	•
Iosi	۲.25	_	10	-	_	0.425	0	K4, K5	10-5	En	V	$I_{os} = E_{12}$	A
(KECOV)	4.25	_	10	-	-	0.425	0	K4,K5	9-11	E13		Your = En	V
Iosi	40	_	40	-	_	-	0	K5	10-5	E14		(RECOV) TOS EM	4
L'eur	40	_	48	_	_	_	0	ķε.	9-11	Ess		Vout = E15	1
RECOV								1111 110			- -	(RECOV)	7
Iph ;	4.25	-	10	_	_	0.425 0.425	1.0	K4, K5	10-5	EIL		Jok = E16 Vour = E17	
NECOV)	425	_	10			0.423	,,,,	1 m 1 m	9-11	\mathcal{E}_{17}	-1-	(RECOV)	V
Ia,	4.25	-	4.25	0	1.4		_	K ₃	12-13	E18		IQ1= E18/2000	my
IGZ	14.2	-	1425	0	1.4	-	-			E19		IQ1 = E19/2000	
Ias		-	41.25	0	1.4	-	-	₩	+	E20		Iq5 E20/2000	•
V 57447			.10	2	-	0.425	-	K4	9-11	\mathcal{E}_{21}		VSTART = E21	V
1	1		1	1							7	<u></u> '	

Table 3.6. Test conditions for 3-terminal adjustable positive voltage regulator (LM117K).

				1	V.	-			101.		,	•	(c. +	u
5	ym\$5.	Test				r	oltag	es	helays	Messa		ı i	Equation	n
'	ĺ			(Vo		<u>. [H</u>		,	Energized			ı — <u>-</u>	•	i
-		VIN	I	1'.	PINS	נחוק		pins	ŀ	, ,	Value	נווח בי		5
	; ··				4.5	6-11	7-2	8.5	None	Hi-Lo		V	V • F	1/
	outs		-5 1500	4.25	0 14.95	_		_	None	9-11	E, Ez	V	Voute Ez	
	0u72	41.2		41.25		_		_			ε_3		Vours: Es	
	oury		-200	41.25	1.95	-	-	_			E4		Voury = E4	•
_	RLINE	_	-	-	-	-	-	_			-		VRLINE = E1-E3	m.
VA		6.25	-5	6.25	0	_	 			_ _	Ē	- -	-	- ' -
V	LOAD	6.25	1500	6.25	14.95	_	_	_ '			E		IRLOADS ES-ES	į
	12040		-	-	-	_	_	-			_		VRLOADE E3 - E4	
	ETH		1500	141:	1495	_	_				E,	V	VATH = De Ez	7
_		4,25		4.25		_	_	_	K2	12-13		m^{V}	IADJ = E8/2000	4 1
7	ADJ	4/.25		4/.25		_	-			1	Eg		IADJ = E9/2000	
	105					<u> </u>						- -	A IAW = Eg-Eg	
(L	IAN INE)	-	_	_	_	_	-	_		_ _		<u> </u>	-INE 2000	
4	TADT	6.25	-5	6.25	0	-	_	-			Eio	'	DIADT : EID-EI	
٨	UAD) I _{ADJ} OAD	6.25	1500	6.25	14.95	_	_	-		ŀ .	\mathcal{E}_{ij}		(LOAD) 2000	
٨	OAD						2416		V11 VC			1	$I_{\alpha} = E_{12}$	·- - -
	051 uT	4.25		10	_	_	0.42S 0.42S	0	K43 K5	10-5			} <i>L</i> /3	',
	ECOV	4.25	_	10	_		0.743		Ky	9-11	£,3		VOUT = E13	•
	osi	40	-	40	_	_	_	0	K5	10-5	E14		JOS EN	·+
	ECOV	40	-	40	-	_	-	0	<i>.</i> . '	9-11	EIS		Vout = E15 (RECOV)	
I	pk	4.25	-	10	-		0.425	1.0	K4, K5	10-5	EIL		Ipx = = = 16	1
Va	ECOV	4.25	-	10	-	-	0.425	1.0	r -	9-11	\mathcal{E}_{17}		VOUT = =17	
P	Q,	4.25	_	4.25	0	1.4	_	_	K ₃	12-13	EIS	Ti-	IQI= E18/2000	11.7
1 .	QZ	14.25	-	14.25	0	1.4	-	-	.]		E19		In= E19/2000	
	Q3	4/.2	-	41.25	0	1.4	-	-	•	+	E20		Iq: E20/2000	•
15	TART	4.79	1500	10	0	-	0 425	-	K4	9-11	\mathcal{E}_{21}	V	VSTART = E21	

(able 3.) Lest condition for 4-terminal adjustable negative voltage regulators (79%).

Synto Te	t d.Tions	App	lied	lest	Volta -Lo]	ges	Relay's Energizes		rement Lines	Equation 4
Vi	I_{L}	PINS	Pins	P.05	Pins	8-2		Pins Hi-Lo	Value Uni	_1
1/5.171 - 8	1 -	- 8	4.99	-	-	-	None	9-11	E, V	Vout = E1 V
Vours -2	0 5	-20	.34	-	-	-			E3 E4	Vour 3 = E3 Vour 4 = E4
10474 -2 10475 -3	5	-30		-	_	-			ES	Vours = Es
10476 -3			.49		_		\	_ _	E	10016 = E6 Y
RLINE - 8	50	-8	.49	-	-	-		!	E	VRLINES = E, - E, mi
VA_1 VB3- 8	1	1	3.49	_	_	_			Eg Eg	VRLINE 2 = E8 - E9
PRINEZ-2		 	3.49					_	<u></u>	RINEZ
1810101 -1		-10	4.99		_	_			E10 E11	V = E10-E11
ALOAD - 1	, 300	-70		_	_	_			-	VRLOADI VRLOADI = E5 - EL
WALCAD -	-		4,00	 			-	- -		
VRTH -15		-15	l			_		1 10	E12	VRTH = E12"
Iscos -1	1	-10	.04		_	_	,	12-13	E13	Isco = E14/2000 A Isco = E14/2000
7 _{50,02} -3		-30			<u> </u>		<u> </u>	-	E14	
(LINE)	1	-8	.04			_			EIS	$\Delta I_{SSO} = E_{IS} - E_{I},$ $(LINE) = \frac{2000}{2000}$
12/04D):-/(500	-10	4.99	_	-	-	+	¥	E16	∆IscD 2 <u>E/3 - E/6</u> (LOAD) 2000 ▼
1051 -10	7 -	-15			-1.0	0	K4, K5	10-5	E17	Iou En A
1(R.500)-11		-15	¦	-	-1.0	٥	2 4 7	7-11	E18	VOUT = E18 V
Ios2 -2	5 -	-30	-	'	2.5	0		10-5	E19	Iosi Eig A
(RSCON-2		-30	-		-2.5	0		9-11	E20	Vout = E20 1
Ioss -3) -	-40	_	_	3.5	0		10-5	EZI	Ios3 Ear A
(RELOW)	s -	-40	-		3.5	0	7	9-11	E22	Vour = = = 22
Ipn -8	-	-15	_	_	0.8		1 - 22	10-5	£23	Ipt = E23. 1
VOUT - 8	-	1-15	-	- •	0.8	i	A - A -	9-11	E.,	Vour = E24 "
Jeony -16	350	-10	3.49		-	-	K1, K2	12-13	£25	Icom = E25/33200 44
VSTART - 8	500	-15	-	_	0.8		K4	9-11	E24	Vout = E26 :
								·		

Table 3-8. Test conditions for %-reminal a vistable negative softace regulators (190).

Symbol	Test	Itions	App.	lied 17s)	Test Hi	Volta Lo]	ges	Relay Energ	/5 9.204		uremei Lines	Ť	Equation	'A 6
	Vin	I.	PINS 1-2	Pins 4-5	Pins 6-11		8-2			Fins Hi-L		units	<u></u>	
Vout 2	- 8 - 8	5		9.99	-		- -	Non	e	9-11	E,	\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\	VOUT 2 = E1	
Vout 3 Vout 4		1000		9.99	_	-	-				E3 E4		Vour 4 = E3	
VOUT 5	-30			.99							Es	-	VOUTS : ES	+
RLINE	-8	100 500	- 8	•99 4.9 9	_	_	-				En En		VRIINE = E, - EL	in
VALINE:	f	500 5	-25 -10	4.99	_	_	-			- -	EIO	- -		
VALOAD VALOAD	,	1000	-10 -	9.99	-	_	1				E,,		VRLOADS = E,O-E,I	
VRTH	-15				-	-	_			-	EIZ		VRTH = E12.	•
Iscos Iscos		5	-10 -3 0	.04	1	_	1 1			12-13	E14		Isco = 513/2000 Isco = 514/2000	ii. 1 !
AISCD (LINE)	i '	5	-8	.04	_		1				EIS		$\frac{\Delta I_{SCO} = E_{IS} - E_{}}{2000}$	1
ΔIscρ (LOAD) IOSA		1000	-10	9.99	-	-1.0	0	¥	ي در	10-5	E16		$\begin{array}{c} AI_{ICD} = \frac{E_{I3} - E_{I6}}{2000} \\ (LOAD) = \frac{E_{I3}}{2000} \end{array}$	P
(RECOV	-10		-15	_		-1.0 2.5	0 0		, , ,	9-11	E18		YouT = E18	
LOSZ L'OUT (RECOU	-25 -25	1	-30 -30	_		-2.5	0	*;		9-11	E20		I 052 E19	
Ios 3	-30 -30		-40 -40	1 1		3.5 3.5	0			10-5	_~'		$I_{OS_3} = E_{21},$ $V_{cur} = E_{22}$	
IPM	-8	_	-15	_		-0.8	_	₹	.	10-5	-		$I_{pk} = E_{23}$	1
VOUT RECOV	-8	-	-15 -10	- 4.99	_	-0.8			5. S	9-11	E 24	<u> </u>	Vour = E24	, U7
ICONY V. TART				7.77	-	-0.8	-	KI,	4	12-1	_ ~	_ _	Icon= E25/33200 Vout= E26	-

The Second section of the first terminal adjustable negative voltage and the control of the second sections.

	r·	<u>.</u> .	,					.,				,	
J., ; : :	Test	•	1 .		Test	BING 7	T	heisys	1	CF 615.61		Equation	1
	Cen	·	. (Vo	lts)		1-20	<u> </u>	Energizes	L			1	1:
1	•	1.		Pins	9105	וחיק	pins		pins		Units	}	
1.	į.			4-5	6-11	7-2	8-2		Hi-Lo		ļ.,	L	
Vours	(17.2) (. e/ s)	! 5 ! c c/	-425		1 -	-	_	None	9-11	E,	IV	Vouri E	1/
Vourz	-4/2	3500 35	4/2			_	_			E		Voutz= E2 Vout 3 = E3	1
VOUTY	4/.2	50			1 -	-	-			Eu		Voury = E4	
IK. IVE		-	1 -	- -	1 -	_	 		<u> </u>	-	-	VRLINE = E1-E3	mV
RLOAD	Į.	ئے ک	F 6 25	0	 		-	-	 - -	Es	 	_	-,-
PRICAD.	•			1	-	_	_	.		E		VRLOADS= E5- E6	
VRLUAD		_	-	-	_	_	_			_		VRLOADE E3 - E4	
RTH	14.6	750	-14.6	7.45	_	-	_		 	E,		VRTH = Dt E)	
IADJ	-4:5	5	-4.25	0	-	_	_	K2	12-13	E	mV	IADS = E8/2000	44
IADS	4/25	5	-41.25	0	-	_	-			Eg		IADJ = E9/2000	
LINE)	-	-	-	_	-	-	-			_		Δ [AW = <u>E8-E9</u> LINE 2000	
A LADS (LCAD)	-6.25	5	-6.25	0	_		-			Eio		DIADS = E10-E11	
ΔΙ ₄₃ (LOAS)	-625	500	-6.25	4.95	-	-	-	¥	'	\mathcal{E}_{II}		(LOAD) 2000	
Tosi		_	-10	_		0.425	0	K4, K5	10-5	E12	V	$I_{os} = E_{i2}$	A
VOUT (KECOV)	-4.25	-	-10	-	- +	0.425	0	Kyns	9-11	E13	.	VOUT = EIS	22
Tosi	- 40	-	-40	-	-	-	0	K5	10-5	E14		IOS EN	4
RECOM	-40	-	-40	-	-		0	A.3	9-11	EIS		Vout = E15 (RECOV)	:'
Ipa			-10	-		0.425		K4, K5	10-5		1	Ipx = E16	.4
VOUT L	4.15	-	-10	-	- †	0.425	-1.0	27.35	9-11	E17		Vout = E17	L.*.
Tai	*25		-4:25		-1.4	-	-	K ₃	/2-/3	E18		IRI= E18/2000	mA
142	142	-	-14.25	0	-1.4	- 1	-			E19		In: E19/2000	
I 43-	41.24	-	41.25	0	-1.4	-	-	₩	y	Ezo		Iq: E20/2000	•
STAAT	4.25	500	-10	0	- ::: }	7.425	- [K4	9-11	\mathcal{E}_{21}	•	VSTART = E21	ک *

Table 3.10. Test conditions for 3-terminal adjustable negative voltage regakators [1113787.]

Symbol	Test	Itoas	App.		Test V	cltag	es	Relays Energized	Measu Sense		Ť	Equation	
	VIN Volti	I_{L}		PINS 4-5	PINS 6-11	Pins 7-2	Pins 8-2		pins Hi-Lo	Value	UniTs		:
Vouts Vouts Vouts Vout4	·41.24	1500 5	-4.25 -4.25 -41.25 -41.25	14.95	l –	-	_ _ _ _	None	9-11	E & & & & & & & & & & & & & & & & & & &	>	Vouti= E1 Vout= E2 Vout 3 : E3 Vout 4 = E4	*
VRLINE	-	-	_	-	-	-	_			-		VRLINE = E1-E3	ii
VRLOAD.	-6.25		-6.25 -6.25		-	- -	-			Es Es		VRLOADI= E5- E6	
RLOAD		_				-			_		-1-	VRLOADE E3 - E4	
VRTH	_	1500		14.95	l -	-		1	*	E,	Y	VRTH = De E7	T
I_{ADJ}	-4.25 -4/.29		-4.25 -4/.25	00	-	-	_ _	K2	12-13	Eg Eg	mγ	$I_{ADJ} = E_{8}/2000$ $I_{ADJ} = E_{9}/2000$	16,4
AIAN (LINS)	-	-	-	1	_	-	-			,	1	$\Delta I_{ADJ} = \frac{E_8 - E_9}{2000}$	
ΔI_{ABJ} (LOAD) ΔI_{ABJ} (LOAD)	-6:25 -6:25		-6.25 -6:25		-	- -	-		- Y	E,	,	Δ IADS = Ε10-Ε11 (LOAD) 2000	7
Iosi	-4:25	-	-10	-	1 1	0.425	0	K4, K5	10-5	En	V	I ₀₅ = E12	4
Vout (RECOV)	-4.25	-	-10	-	_ 1	0.425		K4. K5		E13		VOUT = EIS (RECOV)	
Iosz Vont (RECOV	- 40 - 40	-	-40 -40	_	1 1	-	0	K5"	10-5 9-11	E ₁₄ E ₁₅		Vout = E15 (RECOV)	,*** ,**
Ipk	-4:25	_	-10	-		0.425	-1.0	K4, K5	10-5	EIL	- -	Ipx = E16.	
VouT (RECOV)	-425	-	-10	-		0.425	-J.D	14 35	9-11	E17		Vour = E17	
I_{Q_I}	.4.25	-	-4.25	0	-1.4	1	-	K ₃	12-13	E18		IQ1= E18/2000	n. i
Iqu	-14.2	i	-/4:25	0	-1.4		-			E19		IN= E19/2000	•
Ias	-₩.ય	-	-4/.25	0	-1.4	~	-	+		E20		IQ3 E20/2000	†
STAAT	-4.2	1500	-10	0	_	0.425	-	K4	9-11	\mathcal{E}_{21}	¥	SMAT = E21	,

TABLE 5.11. Summary of 5-5200 jest Adapter Accuracies.

		1,1m	its	Requi	ired ccuracy	S-3260 Basic Meas. Accuracy	S-3260 Test Result	
Parameter	- device		Rign	10:1	4: i	1/		Units
	1M1∋/a, K			.2.5	16.25	126.2-26.3	13.4-3.5	πV
VOIT 1-VOIT4	[1.8947H, K	-1.200V	-1.300v	1 . 5	12.5	20.2-26.3	3.4-3.6	
VELINE	1.01379, K 1.01179, K		+9	9	2.25	·52.4-52.6	· .42	
VRLOADI	LM137H, K	-h	+6	·0.6	1.5	+52.4-52.6	.42	
V RLOAD2	LM137h, K	-t, -3,5	+6 +3.5	·.6	-1.5	·52.4-52.6	·.42	
VRTH	LM13/H, K LM117H, K	-5 -5	+5	1.5	·1.25	· 52.4-52.6	+ .42	
[AD,] l	LM137н, К	+25	+100	6.2	±15.6 +14.38	+.425800 375800	·.007014 ·.005014	uA.
IAD.12	LM137H, K	+25	+100	16.2	15.6	· .425800	·.007014 ·.005014	
DIADJ1	LML37H, K	-5 -5	+5 +5	5	1.25	.85-1.6 75-1.6	·.014028	
DIADJ2	LM137H, K	-5 -5	+5 +5	1.5	÷1.25	7.85-1.6 7.75-1.6	±.014028 ±.01028	
IOSI & IPEAK	LM137H LM137K LM117H LM117K	500 1500 -1800 -3500	1800 3500 -590 -1500	+65 -100 +65• +100	162.5 250 162.5 250	725-6.98 +7.25-7.45 725-6.98 	+.725-6.98 +7.25-7.45 +.725-6.98 +7.25-7.45	mA
TOS 2	LM137H LM137K LM117H LM117K	50 200 - 500 - 800	500 800 -50 -200	+22.5 +60 +22.5 ±30	+56.25 +75 +56.25 +75.0	±.16725 7.7476 1.72516 1.7674	±.16725 ±.7476 ±.72516 ±.7674	
IQ1, IQ2	LM137H, K	.200 -3	3 500	± 140 ± 125	±350 ±312.5	±3.5-40	±.37-1.54 ±3.76-0.4	uA
1Q3	LM137н, к LM117н, к	1 -5	5 -1	± 200 ± 200	± 500 ± 500	±30-50 ±30-50	±3.6-4.15 ±4.15-3.6	

NOTES: $\underline{1}/$ "S-3260 Basic Meas. Accuracy" indicates the accuracy obtainable using the S-3260 test system to measure the parameters directly.

 $[\]frac{2}{}$ "S-3260 Test Result Accuracy" indicates the accuracy obtained using external circuitry and external measurement equipment under S-3260 control.

UN175 10 MAY 79 HI-LIMIT 2.000∪ -15.00U -588.04 -58.064 -58.064 -588.04 5.0000 3.500m 5.90en -15.00U 1.300 9.8 3.5001 -1.697M -57.38U -58.160 -771.eN -861.0N -1.3724 -1.6854 -3.8324 6.334R 4.298H -1.810H 1.243 DEG C Z ×S S.429H -4.750Az -1.255 -280.04 1.250 1.250 -1.227H -1.498H -3.202H -1.357M 678.7∪ -510.5N -45.99n -43.53U 25 -533.5N ▼ N/S 1.225 POS. ADJ. UOLTAGE REGULATORS-LM117H, TEMPERATURE: -2.488H -768.0N 6.334M -1.816H 2.941R -57.58U -1.395a -1.713a -3.875a -56.82U -762.5N 20000 40000 40000 -1.244H -593.0N -1.2987 -1.5687 -3.4428 -1.47**e**M -50.07U -785.8N 5.316A 3.619M -48.48n 1.242 Z -1.1887 -1.4407 -2.9887 -1.470H -496.0N 5.203H 2.715M -1.697H -41.48U -41.97U -575.0N 1.229 LO-LIMIT -9.00m -3.500H -190. OU -100.0n -5.888U -3.50em -5.000U -5.000H 24.1.45 27.41.45 24.1.45 UF-+1.00 UF-90 UF-80 -58 ş CONDITION URTH +41.25 RECOU. +46.00 RECOU. RECOU. RECOU. +4.25 +41.25 +6.25 +1+ +1+ -14-25 -14-25 URLOAD2 +41.25 +4.25 •41.25 **. 25 PARAPETER APLOAD1 LABLI TABLIA TABLIA CLINE CLINE CLINE CLOAD URL INE 20072 20072 20172 20172 20172

NOTE . I UF-FORCING UGLTAGE ON OUTPUT OF DEUICE

	POS. ADJ. VOLI	VOLTAGE	REGULATO	REGULATORS-LM117H;	_	TEMPERATURE:	SS	DEG C ;	10 MAY	62 /
-5.50 -5	-		LO-LIMIT	9 × /S	S/N 7	8 N/S		5/N 10	HI-LIMIT	T CMIT
-5 -5.6001 -731.7U -3.167H -2.828H -3.167H -2.528H -3.167H -2.828H -3.167H -2.520H -3.167H -2.520H -3.167H -2.520H -3.167H -3.167H -3.200H -3.200H -3.200H -3.200H -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -43.18U -47.31U -57.20U -47.20U -47	* * * * * * * * * * * * * * * * * * *		2233 NAVA	aaaa yinne Aune nome	2-6-4 NAMA NAMA		2 0	 ທທ່າທີ່ ພິທີ 4 ພິທີ	######################################	>:->>
+41.25	1; XX		-0.0	6.4478	6.108M	5.429H	4.977H	6.1 98 M	. e	>
+41.25			-3.50em	-791.70	-3.167H	-2.828N	-3.167H	-2.036H	3.500	> =
+41.25 -125 +4.25 -5 +4.25 -5 +4.25 -5 +4.25 -5 +4.25 -5 +4.25 -5 +4.25 -5 -5.000 -53.910 -57.200 -43.18U -47.87U -9 +4.25 -5 -5.000 -58.000 -43.68U -47.87U -9 +4.25 -5 -5.000 -58.000 -43.68U -47.87U -9 +4.25 UF-0U -1.240 -1.215 -1.220 -1.220 +4.25 UF-0U -1.240 -1.215 -1.220 -1.220 +4.25 UF-0U -1.240 -1.220 -1.220 -1.220 +4.25 UF-1.4U -2.200 -1.220 -1.220 +4.25 UF-1.4U -3.000 -1.240 -1.220 -1.220 +4.25 UF-1.4U -3.000 -1.240 -1.220 -1.220 -1.220 +4.25 UF-1.4U -3.000 -1.240 -1.220 -1.			-3.50em	-1.583#	-1.8104	-1.8104	-1.8104	-1.697#	3.500	>
+4.25 -5 -100.0U -53.91U -57.20U -43.18U -47.31U -54.25 -5 -5 -100.0U -54.60U -58.00U -43.68U -47.87U -54.25 -5 -5 -5 -60U -58.00U -497.0N -560.0N -6.25 -5 -5 -5 -5 -5 -5 -5 -5 -5 -5 -5 -5 -5	+41.25	20. 20. 20. 20. 20. 20. 20.	-5.0001	3.619M	2.149M	3.28 0 f	3.054M	3.0548	5.9	>
+4.25 -5 -5 -600 -54.600 -58.000 -43.680 -47.870 -41.25 -5 -5 -5 -5 -5 -5 -5 -5 -5 -5 -5 -5 -5		Υp	-100.0U	-53.910	-57.2 9 U	-43.180	-47.310	-51.3 0 U	-15.00	• «
+4.25 -5 -5 -5 -691.5N -866.9N -497.9N -560.0N -41.25 -5 -5.000U -737.5N -764.5N -593.0N -624.0N -624.0N -624.0N -624.0N -764.5N -593.0N -624.0N -624.0N -624.0N -624.0N -1.250 -	+	'n	-100.00	-54.60U	-58.00n	-43.68U	-47.870	-51.940	-15.00r	« —
#6.25			-5.000U	-691.5N	-8 96.9 4	-497.0N	-560.0N	-641.0N	S.000L	•
# 4.25 UF = 0 UF = 0 UF = 0 UF = 1.20		'	-5. 000 U	-737.5N	-764.5N	-593. 0 N	-624.0N	-682.5N	2.000U	∢
RECOU. 1.256.00	+4.25		# C C C C C C C C C C C C C C C C C C C	-1.240	-1.215	-1.290	-1.220	-1.240	-500.00	
RECOU. 1.245 -1.216 -1.226 -1	+40.00		-500.04	-0.00	-196.	-285. -285. -285.	-210.0H	-236.91	-50.00	-
UF+1.40 -3.000M -1.440M -1.347M -1.137M -1.5602M -1.5602M -1.5602M -3.017M -3.3807M	# . 25 RECOU.	UF=+1.			1.1. 8.0. 8.0. 8.0. 8.0. 8.0. 8.0. 8.0.	7 % C	1.1. 1.0.0. 1.0.0. 1.0.0.0. 1.0.0.0.	1.050	-586. 1.300	787
. ccc. p.c., csc. a.c., a.c., ass. 25.	+14.25 +11.25 +11.25	555		-1.4463	-1.3473 -3.9633 -8.9633	-1.1877 -1.0867 -0.0177		-1.5833 -1.5833 -3.5153	-500 -500 -500 -500 -500 -500 -500 -500	238
T 199.7 KINET DEN'T PEN'T I PAR'T I	+4.25	-5	1.20	1.240	1.258	1.219	1.222	1.227	1.300	· ·

NOTE 11 UP-FORCING VOLTAGE ON OUTPUT OF DEVICE

	v					• •								
0	LIMIT UNITS	2223	3	>	>	>	Œ	Œ	Œ	Œ	47	£747	444	; >
10 MAY	H LIMIT		23.8	12.00	12.00	S. 000m	-15.00U	-15.88U	5.000U	5.0000	-500.0F	1.300 1.300 1.300	-500.0U	1.30
peg c ;	. N.	 	4.977H	1.018H	-1.0187	5.316Mx	-45.740	-46.550	-816.0N	-1.728	1.315	, voice :	-1.0537 -1.463 -3.6728	1.240
-55	7 2/5	2227 20000 20000 20000	4.185A	-2.036A	-1.0189	1.8194	-35.320	-38.240	-2.9210	-1.1650	-1.265 1.265	1.0.4. 1.0.4. 1.0.4. 1.0.4. 1.0.4.	-987.5U -1.2938 -3.1428	1.289
TEMPERATURE:	× × ×	######################################	4.977M	05.8L9	~1.131R	3.9594	-46.590	-49.920	-3.3310	-1.573U	1.228	- 1. 2. 2. 2. 2. 2. 2. 2. 2. 2. 2. 2. 2. 2.	1. 1. 1003 1. 1. 1003 1. 1. 1003 1. 1. 1003	1.239
	5 K/S	 	4.977H	791.8	-964.90	4.5248	-48.56U	-44.75U	-4.19 6 U	-1.455U	1.075	1	-1.0487 -1.3077 -3.3697	1.240
REGULATORS-LM117H;	1 1/8	2222 4444 2444 2444	4.637H	964.90	-791.BU	4.18SM	-33.880	-34.40D	-523.5N	-1.1410	1. 1.000 1.0	1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.	20.00 20.00	1.230
REGULATO	רס-רושוג		-23.00F	-12.00m	-12.00m	-5. 993	-196.9u	-100.0U	-5.000U	-5.888U	-1.800 1.000 000 000	000 000 000 000		1.200
VOLTAGE		È MANA E MANA E MANA	ķ			-125 20.5flaec.)	ķ	è.	ř	-5. -5.00	UF-8U		54.1.4 4.1.4 54.1.4	-500
POS. ADJ. UOLTA	-	* * * * * * * * * * * * * * * * * * *	44. 20.2	%	+41.25	URTH +41.25	+4.25	+41.25	14.25	÷ .25	+4.25 RECOU.	RECOU.	444 2500 2000	+4.25
Pos.	PARAMETER	17002 17002 171002 1717002	URLINE	URLOADI	URLOADS	URTH (IL APP	IABUS	IABJO S	DIADI	plebj2 (Loab	_	PENT.	100 100 100 100	USTART

NOTE 11 UP-FORCING UDLTAGE ON OUTPUT OF DEVICE

Table 3.13. (cont'd).

POS. ADJ. UOLT	UOLTAGE		REGULATORS-LM117H;	-	TEMPERATURE:	-55	DEG C 1	10 AAY	23
PAPAMETER CON	5	LO-LIMIT	9 × × 9	5/N 7		8 × 8	S/N 10	H1-L1M14	ST175
- + + + 	(2222 2000 2000 2000 2000 2000		 		7>>>
URLINE +4.25	ķ	-23.00m	5.429R	S. 768H	4.4118	4.298H	4.637H	23. een	٥
URLOAD! +6.25	9	-12.00	1.6978	452.40	-226.30	-339.30	339.40	12.001	>
URLOADE +41.25		-12.00H	-791.8U	-964.8U	-964.90	-904.8U	-904.90	12.00m	>
URTH +41.25	-125 R 20.58sec.)	-5.000	5.20341	3.28 0 ff	4.298H	4.185ff	4.672A	S. 9994	>
+4.25	Ģ	-10.00	-44.46U	-45.420	-34.630	-38.250	-40.850	-15.00U	Œ
+41.25	Ņ	-190.9U	-45.670	-46.58U	-35.29U	-38.8en	-42.730	-15.00U	α
	ņ	-5.000U	-1.2040	-1.165U	-657.5N	-613.0N	-1.873U	2.000	σ
(LOAD) +41.65 DIADJ2 +6.25 (LOAD)	\$- \$\text{0}\$	-5.000U	-1.438U	-1.693U	-1.305U	-1.3610	-1.499U	5.000U	τ
+4.25	UF-80	-1.800	-1.255	-1.215		-1.255	-1.250	-569.0F	Œ;
++0.00 -+0.00	UF -00	-500.	-0-0-1 -0-0-1	-270.0H		3000 0000 0000 0000	-310.07	-50.00H	,
IPEAK +4.25 (VOUT) RECOV.	UF-+1.00	200 N	-1- -1.55 -1	-1.255 -1.255		-1.855 1.855 1.855		-500.0m	×9×
****	200 11111 1444	444 444 444 444 444 444 444 444 444 44	-1.1538 -1.5508 -3.6628	-1.602H -3.922#	-892.5U -1.1738 -2.9108	-978.5U -1.888H -3.512H	- 995 - 1 - 3488	-560 -560 -560 -560 -560 -560 -560 -560	२१र
USTART +4.25	-5	1.20	1.24	1.253	1.225	1.227	1.229		>

NOTE IS UF-FORCING UGLTAGE ON OUTPUT OF DEVICE

P05.	ADJ.	UOLTAGE	REGULA'	REGULATORS-LM117H	•	TEMPERATURE:	125	DEG C ;	10 MAY	. 62
PARAMETE	œ	CONDITION	LO-LIMIT	S/N 1	S/N	S/N 3	4 N/S	S K/S	MI-LIMIT	STIM
00000 00000 00013	++++ ++44 >44+4 NUMN	ENGNG EIGIN	0000 0000 0000		**************************************	~~~~ 	 			>>>>
URLINE	+4.25	ņ	-23.00H	6.4478	6.673M	7.691M	7.352H	8.031R	23.00m	Þ
URLOAD1	+41.25		-12.00H	-4.411H	-3.619M	-4.637H	-7.126M	-5.542H	12.00H	>
URLOADS			-12.00M	-2.601M	-1.697M	-2.715M	-2.602M	-2.828M	12.00m	
URTH (IL AP	+41.25 LIED FO	-50 -125 R 20.5Msec.)	-5.000M	2.375M	2.8281	1.810M	678.7U	2.9418	5. 000H	>
IADJI	+4.25	Ş	-100.0U	-46.20U	-54.350	-62.68U	-47.690	-64.080	-15.00U	Œ
(LINE)	+41	ř.	-100.0U	-46.630	-54.910	-63.410	-48.160	-64.890	-15.00U	Œ
CLINE) DIADJ1	7	Ş	-5.000U	-435.5N	-555.0N	-728.0N	-473.0N	-720.0N	2.0000	Œ
CLINE) DIADJ2 (LOAD)	+41.25	-500	-5.0000	-189.5N	-286.5N	-274.0N	-103.0N	-325. 0 N	S.888U	٠.
1051 (10017) 1052	+4.25 RECOU. +40.80	UF-8U	-1.800 1.200 -500.03	-1.165 1.221 -280.0M	-1.185 1.239 -200.0M	-1.150 1.233 -195.0M	-1.200 1.215 -310.0M	-1.220 1.243 -190.0M	- 566.0M - 366 - 56.86M	₫ Þ < ;
LIPEAK (VOUT)	RECOU. +4.25 RECOU.	5	-1.800 1.800 1.800		-1.253 -1.1853 -1.035	1.249 1.233	-1.233 1.285 1.214	-1.256 -1.50 -1.50 -1.50	1.388 1.388	4 >
1021	+14.25	UF-+1.40	-3.0000 -3.0000 -5.0000	-1. -1.0.0. -1.0.4 -1.0.4	-1.4283 -1.6833 -3.3423	-1.583H -1.850H -3.793M	-1.382H -1.648H -3.128H	-1.560H -1.832H -3.730H	-500.0U -500.0U -1.0003	ŒŒ
USTART	+4.25	-500	1.200	1.219	1.236	1.230	1.214	1.240	1.366	٠.
P05.	ADJ.	VOLTAGE	REGULATORS-	TORS-LM117H	-	EMPERATURE:	150	DEG C ;	10 MAY	50
PARAMETE	œ	= =	LO-LIMIT	S/N 1	S/N	S/N 3	4 X/S	S N/S	HI-LIMIT UNITS	UNITS
1000	UIN -6.25	ILCHA)	1 2.200	1.227	1.244	1.248	1.223	1.251	1 300	>

NOTE 11 UF-FORCING UOLTAGE ON OUTPUT OF DEUICE

Table 3.14. (cont'd).

Pos.	₽D7.	UOLTAGE	REGULATO	REGULATORS-LM117H;		TEMPERATURE:	125	DEG C ;	10 AAY	49
PARANETER	-	CONDITION	LO-LIMIT	9 ×/8	S/H 7	\$/\$	6 × 8	S/N 10	HI-LIMIT	2115
2555 2555 2555 2555	Z Z Z Z Z Z	*****	3333				2222 9099 6-80 1-80 1-80	HAMA MANA MANA MANA MANA MANA MANA MANA	****	>>>>
UPLINE	X)	ŗ	-23.00m	7.691#	7.0134	7.239R	6.56em	7.8847	23.00m	>
UNICADI	ex:		-12.00m	-2.71SH	-4.75em	-5.882H	-6.447M	-5.882H	12.00	>
URLOADS	2 +41.25		-12.00m	-2.262H	-2.488H	-2.602H	-2.601M	-2.602H	12.00	>
	URTH +41.25	-125 R 20.54sec.)	-5.000	2.6018	1.131#	2.71SH	1.923M	2.036A	S. 8	>
I SOLI	.	Ş	-100.00	-59.25	-63.370	-47.44U	-51.910	-56.66U	-15.9€∪	∢
12012	+41.25	'n	-196.9U	-59.9 9 U	-64. 96 U	-47.910	-52.400	-57.3 0 U	-15.00U	∢
DIADJI		ķ	-5.000U	-653.5N	-688.5N	-466. 0 N	-493.5N	-635.0N	5.9990	σ
DIADJ2 (LOAD)		S- 508-	-5.000U	-296.5N	-238.5N	-208.5N	-208.5N	-220.5N	S. 000U	•
1051 (VOUT) 1052	#4.25 PECOU.	UF-00	-1.886 1.086 -580.67	-1.000 1.036 -215.64	1.249 1.249	-1.00 1.00 -31%-62	1.150 1.212 -205.0H	-1.200 1.218 -235.04	-500.0F	4> 4
	#600.	UF-+1.80		1.251 1.235	1.266 1.266 1.249	-1.00.1 -1.00.1 -2.00.1	-1.145 1.211	 	-500 00 1.000 1.000	~ ~>
	**************************************	25. 1.1.1. 1.1.1. 1.1.1.	\$55 \$33 mmin		-1.507# -1.846# -3.765#		-1.375H -1.667H -3.800H	-1.443# -1.787# -3.456#	-596.9U	e
USTART	.	-5.0	1.20	1.233	1.247	1.206	1.210	1.215	1.38	. >
Pos.	ADJ.	VOLTAGE	REGULATO	REGULATORS-LM117H;		TEMPERATURE:	150	DEG C 3	10 HAY	8
PARAMETER	٠. '	=	LO-LIMIT	S/N 6	5/3 7	8 × × ×	8/8	S.N. 10	HI-LIMIT	2112
2 1000	z K S y	17. 19. 19.	= 1.800 = 1.800	1.225	1.225	1.225	1.226	1.225	1.300	>

NOTE IS UF-FORCING UGLINGE ON DUTPUT OF DEVICE

TABLE 3.15. POS. ADJ. VOLTAGE REGULATOR - LM117H $T_{\rm A} = 25^{\circ}{\rm C}$

6-15-79

PARAMETER	CONDITIONS	LO - LIMIT	S/N7	S/N8	6N/S	S/N10	HI - LIMIT	UNITS
A V _{IN}	$V_{IN} = 6.25 \text{ V}$ $e_{I} = 1 \text{ V}_{RMS}$ $e_{I} = 2400 \cdot \text{Hz}$ $e_{IL} = -125 \text{ mA}$	9	08 ^	۸ ۸	8 7	۸ ۸		dB
V _{NO}	$V_{IN} = 6.25 \text{ V}$ $I_{L} = -50 \text{ mA}$	-	100	95	100	95	120	uVRMS
△ V _{OUT}	$V_{IN} = 6.25 \text{ V}$ $\triangle V_{IN} = 3.0 \text{ V}$ $I_L = -10 \text{ mA}$	-	1.6	2.0	1.6	1.6	9	u//vm
↑ V _{OUT}	$V_{IN} = 6.25 \text{ V}$ · $I_L = -50 \text{ mA}$	-	.20	.20	.20	.18	9.0	mV/mA

6-15-79 (cont'd). $T_A = 25^{\circ}C$ Table 3.15. POS. ADJ. VOLTAGE REGULATOR - LM117H

PARAMETER	CONDITIONS	LO - LIMIT	S/N1	S/N2	S/N4	S/N5	S/N6	HI - LIMIT	UNITS
A VIN	$V_{\rm IN} = 6.25V \\ \boldsymbol{G_1} = 1 \ V_{\rm RMS} \\ \boldsymbol{G} 2400 \ Hz \\ \boldsymbol{I_L} = -125 \ \boldsymbol{mA}$. 99	%	۸ 80	80	80	08 ^	•	dB
VNO	$V_{IN} = 6.25 \text{ V}$ $I_L = -50 \text{ mA}$	ı	100	100	95	100	100	120	uVRMS
A VOUE	$V_{LN} = 6.25 \text{ V}$ $\Delta V_{LN} = 3.0 \text{ V}$ $I_L = -10 \text{ mA}$	-	1.6	1.6	1.6	1.6 2.0	1.6	9	N/Vm
△ V _{OUT}	$V_{IN} = 6.25 \text{ V}$ $I_{L} = -50 \text{ mA}$ $\Delta I_{L} = -200 \text{ mA}$	-	.25	.20	.20	.19	.18	9.0	mV/mA

P05.	POS. ADJ. UOLT	UOLTAGE	REGULATO	REGULATORS-LM117K;		TEMPERATURE	25	DEG C ;	10 AA	73
PAPAMETER	=	=	LO-LIMIT	8/N 1	5 N/S	S.N.3	5/H 4	5 N.S	H: [[M]]	LINIT WITS
0000 0000 1000 1000 1000 1000 1000 100		7378	****		riving St. 1	2222 10040 2004	4044 4044 4044	1144 1144 1444 1444 1444 1444	****	>>>>
WEL INE	+ + + + + + + + + + + + + + + + + + +		-9. ee	3.9598	4.29 8 H	3.506#	6.221M	4.072H	9.	>
URLOAD1 URLOAD2			-3.5007	-1.8161	565.5U -1.81 9 fi	452.40	-1.131M -2.715M	-339.40	3.5004	> >
CRT 20	URTH +41.25	-200 -500 R 20.5Hsec.)	-5.000#		4.637H	3.286	2.036A	2. 488#	5.000	>
1,40,1	+4.25	\$-	-100.0U	- 26.66U	-56.1 9 U	-52.020	-54.310	-59.98U	-15.00U	<
7AD32	+41.25	un I	-100.00	65.05	-56.470	-52.290	-54.830	-60.340	-15.00U	<
DIADII	**************************************	5-	-5.000∪	-392.0N	-373.SN	-276.0N	-513.5N	-357. 0 N	5.0000	•
DIADJS (LOAD)		-5 -1500	S.000U	-214.5N	-272.5N	-152.0N	-63.50N	-141.0N	5. 666 U	<
10051 10050 10050 10050 10000 10000	PECOU. PECOU. PECOU. PECOU.	UF=-0U UF=+1.0U	2-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1		4.44.44.44.44.44.44.44.44.44.44.44.44.4			ก่ → 4 → ก่ → เก → 6 → ก่ → เก → ก่ ท่ ท่ ท่ ผ → เก ท่ ผ → ผ ա ⊕ ш ⊕ ฒ ⊕		4>4 <i>x</i> 4>
101 102 103 USTART	44.25 41.25 41.25 41.25	UF -+1.40 UF -+1.40 UF -+1.40	EEE 0	-1.37em -1.75em -3.845m	-1.9923 -3.9693 1.249	1.0886 1.3886 1.3886 1.8868 1.898	-1.174 -1.5437 -3.5938	1.4433 1.92683 1.0463		. 444 ;
	•								•	

NOTE 11 UF -FORCING VOLTAGE ON OUTPUT OF DEUICE

POS. ADJ. UOLTAGE REGULATORS-LM17K; TEMPERATURE: 25 DEG C ; 100 markerer continuous to the continuous	10 3	ST IN	>>>>	>	>	>	>	Œ	∢	₫	Œ	<i><p< i=""><<i>P</i><<i>P</i></p<></i>	रदर
### CONDITION LOLINIT \$ 1,000 1,000		3 41 11 14	9999	9.6	3.500M	3.500H	S. 000H	-15.00U	-15.00U	2.000	2.000∪	000000 000000 000000 000000 000000	-590.00C
### CONDITION LO-LINIT \$/N 6 \$				3.959M	•	-2.375#	2.828#	-59.320	-59.710	-388.5N	-160.0N		-1.413# -1.762# -3.969#
### CONDITION LO-LINIT \$/N 6 \$	ERATURE:	# X\S	4444 4444 4644	3.393A	-452.40	-2.262M	1.81 01	-55.180	-55.510	-326.5N	-114. 0 N		-1.6832
## CONDITION ***********************************	-	6/N 7		4.298H	Ses . Su	-2.149H	4.298M	-52.190	-52.52	-336.5N	-166. 0 N		-1.3678 -1.6738 -3.5688
## CONDITION ***********************************	RS-LM117K	9 1/9		4.4118	-339.40	-2.149H	3.0548	-56.09U	-56.42U	-330.5N	-168.6N		11.1757 11.15537 13.15137
## CONDITION ***********************************	REGULATO	LO-LIMIT.	3333	-9. 89	-3.500m	-3.500M	-5. 000 ¶	-100.00	-100.0U	-5.88eU	-5.00eU		200 000 000 000 000 000
2 xxxxxx xxxx xxxx xxxx xxxx xxxx xxxx		T104	2 4 9 4 9 1 9 1 9 1 9 1 9 1 9 1 9 1 9 1 9	ý	, S-		-596 -596 20.58sec.)	Š.		ç	-1500	UF-8U UF-8U UF-+1.8U	555
• • • • • • • • • • • • • • • • • • •	ADJ. C	•	2 4 4 4 5 4 4 4 4 5 6 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	Z.		+41.25		+4.25	-41.25	44.25			***** *****
		PARAME :	00011 00011 10011	URLINE	VALOADI	9810402	URTH (SL APP	170		DIAD	019632 (1090)		

NOTE IS UF-FORCING VOLTAGE ON OUTPUT OF DEVICE

STIM 10 MAY 79 HI-LIMIT 12.00H S. 908H 5.000U 23.00H 5.000U -15.88U 12.00N -15.00U DEG C , S'N S 2.488H 678.SU 3.1678 -369. ON -2.675 -575.07 -2.135 -1.122H -1.463H -3.707H -197.0N -791.8U -50.420 -50.620 -276.**0**N -45.110 -375.5N -2.680.0M 4.637H 452.40 -1.810H 2.941H -935.0U -1.428M -3.613M -55 -45.49U 244v 1.240 POS. ADJ. UOLTAGE REGULATORS-LM117K, TEMPERATURE: 1.3574 -163.0N 2.828H .Se5.5U 4.298H -377. ON -43.88**U** -44.04□ 1.240 -234.5N -1.13 -1.60 -3.79 -3.79 3.167# 1.244R -678.70 4.864H -46.290 -46.520 -535.5N 3.28eA 1.357A 644.4244 644.4244 644.4244 -384.SN -509.5N -1.675H -1.525H -3.752H -339.4U 4.185M -45.080 -45.46U 20000 24000 24000 1.245 . I/S -23. -12. -12. LO-LIMIT -5.000U MUN *** -5.00m -5.000U -100.0U -196.9U 1.20 -1500 -1500 -150 -500 20.500 44. 41.1. 41.1. 41.1. UF-+1.8U IL CRA UF - 0U -1500 UF-80 -1500 PARAMETER CONDITION URTH +41.25 +4.25 +60.00 PECOU. PECOU. PECOU. +41.25 URLOADE +41.25 +4.25 URLOADI URL INE INDUI INDUI INDUI CLINE CLINE CLINE CLINE CLINE CLINE CLINE CLINE

NOTE : UF - FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.17. (cont'd).

Pos.	POS. ADJ.	VOLTAGE	REGULA	REGULATORS-LM117K,		TEMPERATURE:	-55	DEG C ;	10 110
PARAMETER	S I	DITION	LO-LIMIT	9 N/S	5		0 × × 0	HI-LIMIT LMITS	UNITS
00011 000111 0001111	**************************************	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				4444 4444 9444	2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.	2000	3335
URLINE	SX.	'n	-23.eem	3.280H	3.3934	2.8284	2.828H	23.00%	. >
URLOAD1	10.5%	9931	-12.00	79.18C	1.697#	113.10	791.80	12.00m	>
URLOADS	02 +41.25		-12.0m	-1.018H	-678.7U	-1.3578	-1.244H	12.00m	>
SE TI	URTH +41.25	-500 R 20.58sec.)	-5.00	3.1679	4.637#	2.488H	3.1678	5.000	>
IADJI	+4.25	۴	-196.90	-46.550	-44.22U	-47.35U	-49.68U	-15.000	∢
IADJA	+41.25	ķ	-18.8	-46.770	-44.45U	-47.56U	-49.9eu	-15.00U	Œ
DIADJI	+4.25	'n	-5. 000 U	-225. 0N	-225.5M	-209.0N	-226.5N	2.000∪	∢
Olabje (Load)		-5 -1500	-5.000U	-320.5N	-389.5N	-286.5N	-371. 0 N	5.000U	Œ
1051 (100UT)	# .25 PECOU.	UF - 9U	1.200		-3.155	-2.59 1.241	-2.7 8 5 1.253	-1.500	Ø
PERCT)	RECOU.	_	1.0.1. 1.0.0.0. 1.0.0.0.0.0.0.0.0.0.0.0.		-755.07 1.250 -2.470 1.247	2	-690.07 1.256 -2.170 1.253	- 28 8 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9	~~~ >
<u> </u>	4.4.4.4.4.3.3.3.3.3.3.3.3.3.3.3.3.3.3.3	55.1. 55.1. 55.1.	444 444 444 444 444 444 444 444 444 44	- 920 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	-1.113H -1.458H -3.449H	-1. -1. 4887 -3. 9. 9. 9. 1	-1.5005 -1.5005 -3.7805	-5500 - 00 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	ववव
USTART	44.25	-1500	1.20	1.246	1.247	1.241	1.253	1.2.6	; >

NOTE 11 UF-FORCING UGLTAGE ON QUIPUT OF DEVICE

Table 3.18.

P05.	ADJ.	VOLTAGE	REGULATORS-	LM117K	1 TEMP	EMPERATURE:	125	DEG C 1	10 MAY	52
PARAMETER		=	LO-LIMIT	S/N 1	S/N	S/N 3	₹ N/S	S N/S	HI-LIHIT	UNITS
2222 2222 2000 11111 11111	++4 ++4 Zununi Runnin	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0000 0000 0000			4444 Mudud Mudud Mudud Mudud Mudud Mudud Mudud Mudud Mudud Mudud	2224 00000 00000 00000	2444 9944 4644 8000		2222
URLINE	+4.25	ıņ I	-23.00m	4.8647	4.864M	4.185M	7.691H	4.864F	23.00H	>
URLOADI	+41.25		-12.00M	-791.7U	-452,40	-1.1318	-2.149M	-1.470N	12.00	>
URLOADS	2 +41.25		-12.00m	-3.506M	-3.054M	-3.167M	-3.733M	-4.411H	12.80M	>
URTH (IL API	URTH +41.25 (IL APPLIED FOR	-180 -500 R 20.5Msec.)	-5.000H	3.054M	4.637M	2.94111	1.8101	1.584#	S.888M	>
IADJI	+4.25	ų	-100.00	-62.27u	- 61. 78U	-56.110	-58.650	-65. 0 2U	-15.00U	Œ
(LINE) IADJ2	7	5.	-100.00	-62.670	-62.201	-56.44U	-59.210	-65.430	-15.00U	σ
(LINE) DIADJ1	7	5-	-5.000U	- 397.0N	-419.0N	-332.0N	-561.5N	-411.0N	2.000∪	α
(LINE) DIADJ2 (LOAD)	+41.25 +6.25	-1500	-5.000U	-5.501N	-85.93N	21.50N	164.5N	61.00N	5.0000	σ
1051 (100UT) 1052		UF-0U	-3.500 1.0000 -1.0000	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	-2.355 1.244 -420.0M	-2.355 -41027 -41027	1.227 1.227 -425.03	-2.095 1.237 -355.0#	-1.500 1.300 -180.01	€> € >
I PEAK (VOUT)		UF-+1.8U		7001 7004	-1.960 1.244	110001	nain	ות∽ונ	1.300	•
1001	+4.25 +14.25 +41.25	0.04 0.04 0.04 0.04 0.04 0.04	-3.686H -3.686H	-1.5455 -1.8663 -3.6963	-1.568# -1.890# -3.750#	-1.4138 -1.6568 -3.3188	-1.207# -1.563# -3.368#	-1.6453 -1.9053 -3.8603	-500.0U -500.0U -1.000M	444
USTART	+4.25	-1500	1.200	1.241	1.242	1.227	1.227	1.238	1.369	>
P05.	ADJ.	VOLTAGE	REGULA	REGULATOKS-LM117K	, TEMP	TEMPERATURE:	150	DEG C ;	10 MAY	23
PARAMETER		CONDITION	LO-LIMIT	1 N/S	S x/S	S/N 3	4 N/S	S N/S	HI-LIMIT	UNITS
vouts	-6.25	11(MA)	1.209	1.242	1.243	25.2	1.238	1.239	1.300	>
				•						

NOTE IL UF-FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.18. (cont'd).

Pos.	ADJ.	VOLTAGE		REGULATORS-LM117K;		TEMPERATURE:	125	DEG C 3	10 MAY	79
PARAMETER	-	-	LO-LIMIT	9 2/5	5.N. 2	8/8	\$ 6	HI LIMIT	T UNITS	
000 000 15 100 15 15 15 15 15 15 15 15 15 15 15 15 15	* + + + + + + + + + + + + + + + + + + +		ววว จ พณะพา	MAMM MAMM AMAA AMAA AMAA			25.45 25.45	9999 9999 9999	7725	
URL INE	25.73	1 5	-23.00H	4.8647	5.429H	4.872M	4.864	23.00M	5	
URLOAD		2.00	-12.00H	-1.697#	J. 191.7U	-1.4704	-1.470H	12.00M	5	
URLOADS	2 +41.25		-12.00m	-3.393#	-3.3938	-3.1678	-3.846H	12.00	>	
WRTH (IL AP	URTH +41.25	-186 -586 R 20.5Msec.)	-5. 80	2.602#	3.8467	1.819	2.036M	5.8004	· 5	
IADJI	+4.25	ķ	-100.0U	-60.31U	-56.22U	-60.10U	-65.18U	-15. 00 U	•	
180.00 180.00 180.00	+41.25	5 -	-100.0U	- 69.69 U	-56.610	-60.440	-65.62U	-15.000	Œ	
DIADI	44.25 25.25	ş,	-5.000U	-383.0N	-388.0N	-343.5N	-438.6N	5.0000	đ	
DIADJ2		-1500	-5.000U	47.00N	-5.501N	50.00N	22.50N	5.0000	Œ	
1051 (VOUT) 1052	+4.25. RECOU.	UF = 60	1.260	1.239	-2.460 1.238		1.248	-1.500	⋖ >	
2. 2. 2. 2. 2. 2. 2. 2. 2. 2. 2. 2. 2. 2	RECOU.					- 4.03.03 - 0.03.03 - 0.03.03 - 0.03.03 - 0.03.03	- 1.05.0 - 1.05.0 - 1.05.0 - 1.05.0 - 1.05.0	- 180 - 1 - 300 -	€2€	
101 102 103 103	+++-25 +14-25 +41-25	UF 11.40	600 600 600 600 600 600 600	-1.3000T -1.6000T -3.380T	1.517		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	15.00.00 1.00.00 1.00.00	- <i>दद</i>	
USTART	** .25	-1500	1.200	1.237	1.237	1.227	1.248	1.30	c 3	
P05.	ADJ.	VOLTAGE		REGULATORS-LM117K;		TEMPERATURE:	150	DEG C ;	10 MAY 7	73
PARAMETER		Ħ	LO-LIMIT	9 · N/S	S/N 7	# × × ×	0 X/S	HI-LIMIT	r units	
VOUTS	-6.25 -6.25		1.200	1.249	1.249	1.249	1.249	1.360	>	

NOTE I UF-FORCING VOLTAGE ON OUTPUT OF DEVICE

6-15-79 $T_A = 25^{\circ}C$ TABLE 3.19. POS. ADJ. VOLTAGE REGULATOR - LM117K

UNITS	dB	uVRMS	Λ/Λw	mV/mA
HI - LIMIT		120	9	0.3
S/NS	08 Λ	105	1.6	•13
S/N4	8 Λ	105	1.6	71°
S/N3	۸ 80	100	1.6 2.0	.13
S/N2	۸ 80	105	1.6	.13
S/N1	۸ 80	105	1.6	.13
LO - LIMIT	59	•	•	•
CONDITIONS	$V_{IN} = 6.25V$ $C_{i} = 1 V_{RMS}$	$V_{\rm LN} = 6.25V$ $I_{\rm L} = -100 \text{ mA}$	$V_{IN} = 6.25V$ $\Delta V_{IN} = 3.0 V$ $I_L = -10 \text{ mA}$	$V_{IN} = 6.25V$ $I_{L} = -100 \text{ mA}$ $\triangle I_{L} = -400 \text{ mA}$
PARAMETER	A VIN	V _{NO}	A V _{OUT}	A Vour

6-15-79 (cont'd). $T_A = 25^{\circ}C$ Table 3.19. POS. ADJ. VOLTAGE REGULATOR - LM117K

			Marin American Articles (Marines Marines Marin	
UNITS	ф	uVRMS	W/V	mV/mA
HI - LIMIT	ı	120	9	0.3
	ı	l .	i	ı
8/N9	۸ ۸	100	2.0	.13
S/N8	٧ 80	105	1.6	.13
S/N7	۸ 80	100	1.6	.14
S/N6	A	105	1.6	. 14
LO - LIMIT		!	1	ı
CONDITIONS	$V_{IN} = 6.25V$ $Q_{i} = 1 V_{RMS}$ $Q_{i} = 2400 Hz$ $I_{L} = -500 mA$	$V_{IN} = 6.25 \acute{V}$ $I_{L} = -100 \text{ mA}$	$V_{IN} = 6.25 \text{ V}$ $\Delta V_{IN} = 3.0 \text{ V}$ $I_L = -10 \text{ mA}$	$V_{IN} = 6.25 \text{ V}$ $I_{L} = -100 \text{ mA}$ $\triangle I_{L} = -400 \text{ mA}$
PARAMETER	△ V _{IN}	VNO	A V OUT	

NEG.	NEG. ADJ. UOLTA	UOLTAGE	REGULA	REGULATORS-LM137H;		TEMPERATURE:	ระ	DEG C ;	91 MAY	23
PARAMETER		Ħ	LO-LIMIT	S/N 1	N X/S	S/N 3	4 1/5	S.N.S	HI-LIMIT	STINU.
0000 0000 11100 11100 11100	1144 1144 2444 24444 24444 24444	11 (34) 5005 5005 5005	าาาา เกลเล่น เกลเล่น เกลเล่น	1111 0000 0400 0400	 	1 1 1 1 1111 0000 0000 0000	1111 1111 1111 1111 1111 1111 1111 1111 1111	1111 2000 4000 4000 4000		>>>>
URLINE	-4.25	ß	-9.000H	-2.715M	~2.262M	-2.262M	-2.375M	~2.375M	9.00eH	>
URLOADI	1 -6.25		-6.880F	12.33ft	10.63MX	10.18Mx	12.78NE	11.65MI	6.00em	>
URLOADS	2 -41.25	96 96 1	-6.000M	1.244M	1.018M	1.131M	1.018M	904.90	6.000H	>
URTH (IL APF	URTH -14.60 (IL APPLIED FOR	750 750 R 10.5Msec.)	-5.000M	452.50	339.30	. 565.50	339.30	678.5U	S.669m	>
IADJI	-4.25	.	25.000	71.940	64.680	64.720	74.77U	70.910	100.00	∢
I PO 12	-41.25	S	25.090	75.33U	67.380	67.430	78.97U	74.28U	100.90	Œ
DIADJI	1,		-5.000∪	3.396U	0.697∪	2.7090	3.3010	3.3690	2.00eU	Œ
OLANE D DIADJ2 (LOAD)		5005	-5.000U	-1.256U	-937.6N	-1.017U	-1.1530	-1.1030	5.000U	Œ
1051 (0001) 1052 (0001) IPEAK (0001)	RECOU. -40.00 RECOU. -4.25	UF-8U UF-8U UF1.8U	500.07 50.007 -1.00.007 500.007 -1.00.007	1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1		11. 11. 11. 11. 11. 11. 11. 11. 11. 11.		1.185 32537 1.2500 1.1850		4>4>4>
1001 1002 1002	-14.25 -14.25 -41.25	2000 FFF FFF FFF FFF FFF FFF FFF FFF FFF	2000 2000 1.000 00.00 000 000	4 60 . 0U 4 80 . 0U 1 . 980#	468.8U 1.866M	488.8U 1.888U	748.9U 810.9U 800.0U	432.0U 508.0U 2.020M	3.0000 5.0000 FER	444
USTART	-4.25	500	-1.275	-1.241	-1.242	-1.243	-1.233	-1.238	-1.200	>

NOTE 11 UF-FORCING VOLTAGE ON OUTPUT OF DEVICE

NOTE 11 UF-FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.21.

NEG.	ADJ.	VOLTAGE	REGULAT	REGULATORS-LM137H;		TEMPERATURE:	-55	DEG C 3	01 MAY	29
PARAMETER		CONDITION	LO-LIMIT	 L \	N £	× ×	¥ 2.5	S N S	MI EIRIT	271.72
2000 2000 2000 144 144 144 144	2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	1L(M) 505 506 506	0000 0000 mmmm 1111	1 1 1 	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1111 MUNIO 441-1-	4400 0000	2	232	2222
URLINE	-4.25	υ'n	-23.00M	-4.637M	-2.828H	-3.9598	-4.637H	-3.733M	23.00H	>
URLOAD:	-4: -6:25		-12.00%	9.275M	8.257M	16.07	8.257#	7.578M	12.00m	>
5000	_		-12.00m	791.8U	678.7∪	1.1318	1.357M	1.244M	12.00m	>
URTH CIL APP		50 750 7 10.54sec.)	-5.000m	-226.3U	0.000	452.4U	-565.50	-791.8U	S. 9994	>
140.11	25.4-	S	25.000	76.92⊍	67.77	78.460	76. 0 SU	72.36U	199.90	Œ
CLINE)	7		25.00	80.40	79.500	81.880	79.49n	75.00U	166.60	Œ
CLINE.		•	-5.000	3.4760	2.729L	3.4230	3.4440	5. 6 35u	S.666U	∢
CLINE) DIADJ2	-41.25	85	-5.006	-1.6040	-1.499⊍	-1.680∪	-1.504u	-1.516U	S.000U	₹
	PECOU. -40.00 RECOU.	5 5 5			4	24 0 0 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1.1.60 4.00 1.1.00 4.00 1.1.00 1		21.01.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.	47 47£7
	-4.25 -14.25 -41.25	200 1111 1111 1111 1111	100 - 000 -	24.0 24.0 26.0 20.0 20.0 20.0 20.0	1.86.60 1.86.60 1.86.60	2428 2488 2488 200 200 300 300	320.00 416.00 2.6134	364.90 1.90.90 1.90.90	EEE 000	888
USTART		985	-1.30	-1.243	-1.245	-1.235	-1.240	-1.249	-1.200	

NOTE: 11 UF-FORCING VOLTAGE ON OUTPUT OF DEVICE

NEG.	NEG. ADJ. UOLT	VOLTAGE	REGULA'	REGULATORS-LM137H;		TEMPERATURE:	£85	DEG C 3	01 MAY	20
PARAMETER		CONDITION	LO-LIMIT	9 1/8	5/R 7	80 N/S	8 N S	S/N 10	MI-LIMIT	UN115
1000 15000 15000 15000	21.44.1 24.44.1 24.44.1 24.44.1 24.44.1	7L (3A) See 5 CS	9999 8699 MONO	1111 4444 6468 8488	1 1 1 1 2 2 2 1 2 2 2 2 2 2 2 2 2 2 2 2	11111 00000 N4 NN NC 888	2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0000 Nana	>>>>
			100 EC-		-3.619H	-3,1678	-3.393#	-4.298H	23.60#	>
UNIT DAD 1	141.25		-12.00H	7.6917	8.935M	9.0498	8.789M	8.596M	12.00H	Э.
UPLOADS	_		-12.00m	1.018	678.5U	791.80	565.5U	1.018#	12.00m	.
SETH CIL AP		50 750 750	-5. 6 00H	-113.10	226.3U	999.	-339.40	113.10	5.000	>
T. D. 11	-4.25	v	. SS.	73.740	74.950	67.670	73.980	79.140	100.00	Œ
(LINE)	•	ı vo	25.000	77.320	77.810	76.220	77.560	82.870	166.60	Œ
(LINE) DIADJ1			-5.000U	3.5810	2.8590	2.5530	3.5820	3.7220	5.0000	Œ
(LINE) DIADJE (LOAD)	-41.25	5	-5.8880	-1.692U	-1.5230	-1.436U	-1.65 0 U	-1.580U	5.6660	σ
1051 (000T) 1052 (000T)	-4.25 -40.60 -40.60 -4.25	UF-6U UF-6U UF-1.6U			24.1.4.1.4.1.4.1.4.1.4.1.4.1.4.1.4.1.4.1	1.4.1. 40.00.00.00.00.00.00.00.00.00.00.00.00.0	1.160 365.0M		2.4.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.	€> € > € >
LOUT 1901 1901	-4.25	25. 1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-	-1.300 -1.300 -000 -000 -000 -000	-1.248 304.0U	-1.245 320.00 416.00	1.64. 904.0U 1.805.8U	11.645 304.0U 400.0U 1.965R	2.6.9U 8.6.9U 8.6.9U	0.000 0.000 0.000 0.000	
USTART		280	-1.300	-1.247	-1.244	-1.246	-1.246	-1.248	-1.200	>

NOTE IS UF-FORCING UOLTAGE ON OUTPUT OF DEVICE

Table 3.22.

NEG.	ADJ.	UOLTAGE		REGULATORS-LM137H;		TEMPERATURE:	125	DEG C ;	61 H A∀	9
BADAM		CONDITION	LO-LIMIT	\$ N.S	S/8	E ×/8	7 2/5	S N/S	HI-LIMIT	T UN175
00011 00017 00017 100017	4 4 1 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4		9000 9000 MMMM 11111		1111 2000 8000 8400 8400	 	44000 04111	 5.5.5.5 6.6.	******	2223
URLINE	-4.25	v	-23.00M	-2.602H	-1.810H	-1.8707	-1.4704	-2.149H	23.00	5
URLOAD	_	70 6	-12.9em	16.17#	12.67#1	16.06Mx	15.61#1	16.17M#	12.00	>
URLOADZ	2 -41.25		-12.00H	1.583H	1.131#	1.357H	1.819	2.149M	12.00	-
CIL AP	URTH -14.60	756 R 10.5Hsec.)	-5. 999 H	S65.5U	964.90	1.018H	1.0187	1.131#	S. 888m	5
16001	-4.25	v	25.00U	76.330	68 .360	79.380	75.98U	72.310	196.90	•
200	-41.25	S	25.00U	79.300	70.920	82.5 0 U	79. 96 U	74.730	100.0U	•
DIADII	4.25	s	-5.000U	2.9710	2.5540	3.1200	3.0758	2.4210	5.0001	₫
DIADJ2 (LOAD)		5 00 5	-5.000U	-604.5N	-513.0N·	-632.5N	-558.0N	-576.5N	S.000U	٩
1051 1052 1052 10017	-4.25 PECOU. -40.00 RECOU.	UF-9U	.1.300 -1.300 -1.3003	24.00.00 24.00.00 24.00.00	11.000 14.000 14.000 14.000 14.000 14.000		1.170 -1.035 315.035	1.0.10 1.0.10 10.00 10.00	2. 800 5.000 6.000 6.000	4>4
IPEAK (UOUT)	-4.25 RECOU.	UF1.0U	-1.300.	1.145			1.170		1.000	76>
 	-14.05 -11.05 -41.05	444 1111 1254	1000 000 000 000 1000	488.61 582.50 1.82.50	448.60.00 1.06.00 1.088	508.00 511.50 1.980F	496.0U 540.0U 1.857R	464.0U 520.0U 1.723	W.W.N.	444
USTART	-4.25	95	-1.300	-1.24	-1.243	-1.232	-1.236	-1.249	-1.200	>
MEG.	ADJ.	VOLTAGE	REGULATO	REGULATORS-LM137H;		TEMPERATURE:	150	DEG C 1	91 HAY	82
PARAMETER		=	LO-LIMIT	S/N 1	S/8	E 4.8	* * * * * * * * * * * * * * * * * * * *	S.'N 5	HI-LIMIT	CMITS
90015	2 M		-1.300	-1.256	-1.256	-1.246	-1.250	-1.266	1-1-200	>

NOTE 11 UF-FORCING VOLTAGE ON GUTPUT OF DEVICE

Table 3.22. (cont'd).

NEG	NEG: ADJ. VOLT	VOLTAGE		REGULATORS-LM137H1		TEMPERATURE:	125	DEG C 1	91 MAY	20
Panume TER		-	LO-LIMIT	9 K S	6/11	# X\S	6 ×/5	5/N 10	MI LIMIT	\$118
2222 2222 1222 1312 1412	1 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	200 00 00 00 00 00 00 00 00 00 00 00 00	****	Andria Andria	MUNION MUN MUNION MUN MUNION MUNION MUNION MUNION MUNION MUN MUNION MUNION MUNION MUN MUNION MUNION MUNION MUNION MUN MUN MUN MUN MUN MUN MUN MUN MUN	1 1 1 1 00000		2		>>>>
URL INE	-4.25	•	-23.001	-1.9234	-1.697H	-1.697H	-2.262M	-2.036H	23. 88	>
URLOADI		un d	-12.00m	13.35Mg	16.51#	15.27H\$	14.14Mg	14.93Mx	12.00	>
WILDADS	2 -41.25	P in (-12.00m	1.4794	1.4704	1.357H	1.697R	1.923#	12.00	>
CIL PP	URTH -14.60	766 766 766 766 766 766	-S. ee	791.80	1.0189	1.0187	678.70	678.7U	S. 8	5
IADJI	-4.25	w	25.9	72.520	74.440	67.070	74.240	79.340	196.90	∢
100 J	-41.25	w	28.eeu	75.560	76.990	69.360	77.420	82.600	100.00	Œ
		w	-5.000U	3.6330	2.5510	2.2910	3.1820	3.2620	5.000∪	Œ
DIABJE	-6.25	S 9 68	-5.000U	-642. 0 N	-572.SN	-5 06.0 N	45.509-	-600.5N	5.000U	σ
1051 (-4.25 RECOV.	UF.0U	-1.300 50.001	1.230 -1.242 330.04	1.220 -1.237 335.0M	1.215 -1.246 330.6M	1.165 -1.243 315.6M	1.175 -1.240 310.0M	1.800 0.000 0.000	4> 4
1450 1450 1500 1500 1500 1500 1500 1500	RECOU. -4.25 PECOU.	UF1.0U	-1.900 1000 -1.900	-1.055 -1.035 -1.045	-1.25.0 0.00.1 0.00.0 0.00.1	-1.056 1.056 -1.056	-1.258 1.170 -1.243	-1.256 1.175 -1.240	-1.000 0000 0000 0000	>4>
1001	41.45 2.25 2.25 2.25	555		248.90. 504.90. 1.7667	5.46.90 5.40.90 5.60.90	. 648 . 64.9U	448.0U 510.0U 1.840H	564.6U 566.6U 1.925R	MUN 999 999	444
USTART	-4.8	85	-1.3e	-1.242	-1.236	-1.242	-1.242	-1.241	-1.200	; >
NEG.	ADJ.	VOLTAGE		REGULATORS-LM137H;		TEMPERATURE:	150	DEG C 3	61 MA ∀	29
PARANETER		=	LO-LIMIT	9 N/S	5/N	S/N	0 K/S	•1 ×/5	HI-LIMIT	271NU
\$1700	2012 2012 2012 2012 2012 2012 2012 2012	IL (MA)	-1.300	-1.256	-1.255	-1.265	-1.865	-1.265	-1.300	>

NOTE 11 UF-FORCING VOLTAGE ON OUTPUT OF DEVICE

 $T_{\mathbf{A}} = 25^{\circ} C$ TABLE 3.23. NEG. ADJ. VOLTAGE REGULATOR - LM137H

UNITS	a b	uVRMS	л/лш	mV/mA
HI - LIMIT	1	120	80	0.3
S/N5	57.7	70	. 38	• 05
S/N4	59.2	70	30	.045
S/N3	60	70	35	*0°
S/N2	57.7	70	36	°05
S/N1	0.09	20	30	• 05
LO - LIMIT	84	1	•	•
CONDITONS	$V_{IN} = -6.25V$ $Q_1 = 1 V_{RMS}$ $Q_2 = 1 V_{RMS}$ $Q_3 = 2400 Hz$ $I_L = 125 mA$	$V_{IN} = -6.25V$ $I_L = 50 \text{ mA}$	$V_{IN} = -6.25V$ $\triangle V_{IN} = -1.0V$ $I_{L} = 10 \text{ mA}$	$V_{IN} = -6.25V$ $I_{L} = 50 \text{ mA}$ $\Delta I_{L} = 200 \text{ mA}$
PARAMETER	A VIN A VOUT	V NO	△ V _{OUT}	△ V _{OUT}

6-15-79 (cont'd). $T_A = 25^{\circ}C$ Table 3.23. NEG. ADJ. VOLTAGE REGULATOR - LM137H

T UNITS	фВ	UVRMS	mV/V	mV/mA
HI - LIMIT		120	80	0.3
S/N10	0.09	70	28	•05
6N/S	59.2	70	30	•00
S/N7 S/N8	58.4 57.0	70	28	50.
S/N7		70	35	°0.5
S/N6	57.4	70	36	.05
1.0 - LIMIT	87	-	•	•
COND IT I ONS	$V_{IN} = -6.25V$ $C_{i} = 1 \text{ VRMS}$ $C_{i} = 1 \text{ VRMS}$ $C_{i} = 125 \text{ mA}$	$V_{IN} = -6.25V$ $I_{L} = 50 \text{ mA}$	$\begin{array}{c} v_{\rm IN} = -6.25 v \\ \triangle v_{\rm IN} = -1.0 v \\ I_{\rm L} = 10 \text{ mA} \end{array}$	$V_{IN} = -6.25 \text{ V}$ $I_{L} = 50 \text{ mA}$ $\triangle I_{L} = 200 \text{ mA}$
PARAMETER	A VIN A VGUT	VNO	A VOUT	A VOUT

UNITS 2222 > 79 **a** 444 D Œ HI-LIMIT 3.000m 3.000m 5.000m 6.808F 30 APR 5.6991 5.6067 9.000F 6.000H 100.00 100.001 5.eeeu -1.225 -1.225 -1.225 -1.225 -1.200 2.715R 4.185M -510.0N 400.0U 560.0U 2.080M 452.40 U5.197 60.140 63.500 3.3580 25.05.0 20.05. ပ DEG 2.328 5.923 1.2533 1.258 2.358 1.558 5.09em 1.1318 1.470M 65.470 -538.5N 352.0U 448.0U 1.720M -2.149M 62.990 2.5700 -1.255 -1.255 -1.259 -1.259 25 1.252 NEG. ADJ. UOLTAGE REGULATORS-LM137K; TEMPERATURE: 2.25.00 2.25.0 -1.923M 4.977H 791.80 1.018M 64.52U 67.09U -272.0N 416.0U 480.0U 1.800M 2.5720 -1.267 -1.268 1.260 N/8 -2.149M 4.864M 1.1318 339.40 67.790 70.510 2.8140 -508.0N 400.0U 480.0U 1.920M 1.253 - 1.25 - 1.55 - -3.506M 4.524M 1.018M 565.5U -669.5N 540.0U 960.0U 2.882M 73.08U 76.620 3.5410 -9.000H LO-LIMIT -5.000M 200.00 200.0U 1.000M 25.000 -5.000U -5.000U -6.000M 25.000 -1.275 -1.275 -1.275 -1.275 -1.275 1500 250 1500 16.58sc.) UF -- 1.45 UF -- 1.45 UF -- 1.45 UF--1.0U S ស UF-90 UF-80 CONDITION URTH -14.60 -4.25 -40.00 RECOU. RECOU. -41.25 -41.25 -41.25 -6.85 -41.25 PARAMETER URLOADI URLOADS 1051 1052 1052 10047) F 10647) F CABUS (ABUS) (ABUS) (ABUS) (LINE) (CABUS) URLINE 00UT2 00UT2 00UT3

11 UF.FORCING UOLTAGE ON OUTPUT OF DEVICE

Table 3.24. (cont'd).

30 APR 73

NEG.	ADJ.	UOLTAGE	REGULAT	REGULATORS-LM137K,		TEMPERATURE:	. S 2	DEG C
PARNMETER	•		L3-LIHIT	S/N 7	2 2 3	8 ×/S	HI-LIMIT UNI"S	S-140
00000 00000 000000 000000 000000	24444 24444	ing N	interests selected			1 1 1 1 111111111111111111111111111111	ราชาชาชา พิพิพิพิพิ พิพิพิพิพิ	>> >>
URLINE	7:	s o	-9.0	-2. 828 H	-2.601H	-1.4708	9.0001	>
URLOADI	6.33	5	-6. eeen	4.750H	4.637H	4.75em	6.9997	>
URLOADE	2 -41.25	2 C	-6.999	113.10	1.2448	904.80	6.990H	>
CIL AP	URTH -14.60	1500 1500 R 10.5Hsec.)	-5.	791.70	1.357H	1.1318	5. 909 H	>
IADJI	4.25	ıs	.X.	70.72U	67.75U	67.39U	196.9U	•
2001	-41.25	w	.×.	73.62U	71.690	70.310	100.0€	Œ
DIADLI	4.25	S	-5.000U	2.9000	3.3430	2.9220	5.6900	<
DIADJ2 (LOAD.	'	5 15 0 0	-S.000U	-538.5N	-598.5N	-518. 0 N	S.000U	Œ
1051	-4.25 RECOU.	UF-80	1.500	2.345	2.275	2.240	3.500	
1000 1000 1000 1000 1000 1000 1000 100	RECOV.	UF1.0U					3.000 1.000	<i>4245</i>
- - - - - - - - - - - - - - - - - - -	-14 -14 -25 -25 -25 -25 -25 -25 -25 -25 -25 -25	25.1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-	205 305 305 305	416.0U 510.0U 1.9824	384. eU 496. eU 1. 9684	444 96.00 1.00.00 1.00.00		
USTART	4.85	1500	-1.275	-1.253	-1.236	-1.245	-1.200	>

NOTE 11 UF-FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.25.

رن رن	S- 145	3355	>	5	>	>	Œ	Œ	Œ	σ	4>	エ プマン	रदर	د :
30 APR	MI-LIMIT		23.00F	12.00#	12.00M	S.888M	190.90	166.6∪	2.000	S.eeeu	3.500	1	WW.	-1.200
4 0 0 W	9 ¥	25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.0000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.000 25.00	-3.733M	3.619m	113.00	452.50	65.080	69.320	4.2410	-765. AN	2.195 -1.257	1.25.01. 1.25.01. 1.25.01. 1.25.01. 1.25.01.	320.00 526.00 2.200 2.200	-1.257
יי ע	, r . x . y	1 0.0000 0.0000 0.0000	-2.828#	3.393₩	07.164	113.00	66.240	69.140	2.9010	-988.5N		-1-256 -1-256 -1-248	272.8U 384.8U 1.787M	-1.249
TEMPERATURE:	7 2/5	MUGO 00 00 00 00 00 00 00 00 00 00 00 00 00	-3.167M	2.488H	452.40	0.000	67.80	7€.86∪	3.0620	-668. 0 N	2.475 -1.253 870.988		320.00 368.00 1.870	-1.252
	€ 13 13 13 13 13 13 13 13 13 13 13 13 13		-3.167#	2.941M	452.40	-339.40	71.940	75.020	3.0810	-873.5N	0.10 0.00 0.00 0.00 0.00 0.00 0.00	-1.257 -1.249	320.0U 416.0U 2.00SM	-1.250
REGULATORS-LM137K;	1. X/S	1 1 1 1 4 4 70 70 6 4 4 4	-S.8827	3.393#	678.7U	-678.7U	77.530	81.080	3.5510	-799.5N	1.00.1.00.1.00.1.00.1.00.1.00.1.00.1.0		400 000 000 000 000 000 000 000 000 000	-1.245
REGULA"	LO-LIMIT	0000 0000 0000 0000 0000 0000 1111	-23. 0 0M	-12.00m	-12.00H	-5.000m	25.00U	25.00U	-5.80eu	-5.60eu	1.500 1.300	1.300	1.000 1.000 1.000 1.000 1.000	-1.300
VOLTAGE	COND: 110N		v	50031		1500 10.5Msec.	S	ſ	v	5 1500	UF-8U	UF 1.0U	UF-1.1.40	1500
ADJ.	=	4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	2	-6.25	-41.25	URTH -14.68	-4.25	-41.25	4.25	140	AECOU.	RECOU.	-14.25 -14.25 -41.25	-4.25
ZEG.	PARAMETER	2000 2000 2000 1000 1000 1000	URLINE	URLOADI	URLOADS	URTH (IL APP	IADJI	140.12	DIADUI	DIADJ2 (LOAD)	1051 (0007 / F	COOUT :	1901	USTART

NUIS IT UNIVERDING NOTINGE ON OUTPUT OF DEUTCE

*! ! 1.25. (cont'd).

30 APR 79

4E.G.	₽DJ.	VOLTAGE	REGULA	REGULATORS-LM137K,		TEMPERATURE:	-55	DEG C	••
Ĭ	3400 W3.1	COMBITION	LO-LIMIT	C N/S	# X\S	0 ×/5	HI-LIMIT UNITS	STINO 1	
3333	A 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	ing in	9999 9666 0000 0000	1 1 1 1 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	1111 	1111 1111 11111 11111 11111	2000	2223	
UPL INE	\$3. 7.	, M	-23.00H	-2.828H	-4.072H	-3.2804	23.00	>	
MICOMDI		un ge	-12.00H	2.941#	3.280	3.506M	12.00M	>	
UNCONDS	2 -41.25		-12.00H	452.40	452.50	964.80	12.9m	3	
CIL APPL	-14.60 PLIED FOR	1500 1500 10.5Msec.)	-5. 999 H	113.10	265.5U	226.30	S. 666 H	>	
IABUI	-4.25	'n	28.9 9 U	74.670	73.120	71.410	100.00	α	
INDIR	-41.25	s	25.000	U78.77	76.710	74.840	100.0U	Œ	
DIADUI	-4.25	Ŋ	-5.000U	3.2010	3.5830	3.4260	5.000U	Œ	
DIADJ2 (LOAD)	-6.25	1500	-5.000U	-866. e N	-847.0N	-851.5N	5.000U	₫	
1051	-4.25	UF.9∪	1.500	92.5	2.2. 2.2.2	5.00	3.500	?	
1052	46.00	UF	200.00	720.05	755.07	715.03	890 800 800 800 800 800 800	> &	
15 15 15 15 15 15 15 15 15 15 15 15 15 1	-4.25 RECOU.	UF1.00	-1 			-1.256 -1.244	-1.000 -1.000	.2 <i>9</i> 2	
	-14.25 -11.25	555 11.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1	1.000 1.000 1.000 1.000 1.000	200 200 200 200 200 200 200 200 200 200	22.00 4.00 4.00 4.00 5.00 5.00 5.00	320.00 424.00 1.9305	MUN.	999	
USTART	-4.25	1500	1-1.300	-1.249	-1.239	-1.244	-1.20	; > _i	

NOTE : 1 UF-FORCING UGLTAGE ON OUTPUT OF BEUICE

NEG.	ADJ.	UOLTAGE		REGULATORS-LM137K	•	TEMPERATURE:	125	DEG C ;	30 APR	20
PARAMETER		=	LO-LINIT	5/X 1	S/N	S/N 4	S ×/S	9 N/S	HI-LIMIT	T UNITS
000111 00013 00013 4	24444 24444 24444 24444	11. (AA) 1500 200 200	6866 6868 MMCH 1111	1 1 1 1 O MOS O MOS	1111 2000 4000 4000	1111 0000 0400 0400	1111 000 000 000 000 000		0000 0000 0000 0000 0000	>>>>
URLINE	-4.25	ıs	-23.00M	-2.941H	-2.262M	-2.036M	-2.036M	-1.697M	23.00M	>
URLOADI	-6.25		-12.00M	7.613H	6.900M	7.013M	7.465M	6.4478	12.00H	>
URLOADS	-41.25		-12.00H	1.3578	904.80	1.1318	1.244M	1.018M	12.00H	>
URTH (IL APP	URTH -14.68 (IL APPLIED FOR	266 1588 R 16.5Msec.)	-S.000H	565.50	1.583#	1.470H	1.923M	1.583M	5.000	>
IADJI	-4.25	v	25.000	77.880	72.680	68.610	66.710	63.200	100.00	Œ
(LINE)	-41.25	s	25.000	81.050	75.330	71.380	69.320	66.140	100.0U	•
(LINE) DIADJ1	-4.25	S	-5.0000	3.1690	2.653U	2.7620	2.6170	2.940U	5.0000	•
OLINE) DIADJ2 (LOAD)	-6.25	1506	-5.000U	-262.5N	-315.0N	-196.0N	-442.0N	-274.5N	S.000U	Œ
1051 (4001) 1052	-4.25 RECOU.		1.500 -1.300 200.03	2.120 -1.253 490.09	51.055 510.08 510.08	-1.200 -1.200 -000 -000	2.686 -1.2551 556.61	-11-12-12-13-13-13-13-13-13-13-13-13-13-13-13-13-	3.500 -1.200 800.0H	ری دن
	RECOU. -4.25 RECOU.	UF 1.8U	-1.300 -1.500 -1.300	-1.25.1- -1.255.	-1.264 -1.2564 -1.256	-1.072 -1.045 -1.065	-1.656 -1.851 -2.851	-1.658 -1.851	-1.686 3.588	* * >
001 1001 100	14.25	. UF1.40 UF1.40 UF1.40	1.000 1.000 0.00 1.000 0.00	8860.00 890.00 8.00U	448.0U 508.0U 1.760H	448.00 496.0U 1.640m	416.0U 480.0U 1.560M	416.0U 570.0U 1.810H	7.0000 0.0000 0.0000 EEE	444
USTART	-4.25	1500	-1.300	-1.254	-1.256	-1.264	-1.251	-1.251	-1.200	3
NEG.	ADJ.	VOLTAGE	REGULATOR	ORS-LM137K	•	TEMPERATURE:	150	DEG C ;	30 APR	29
PARAMETER	•	~	LO-LIMIT	~ × ×	2 ×/9	4 × × ×	S ×× S	9. N.S	HI-LIMIT	UNITS
. STUON	-6.25 -6.25	(4E) 11	-1.360	-1.260	-1.262	-1.271	-1.258	-1.256	-1.200	>

NOTE : 11 UF-FORCING UOLTAGE ON OUTPUT OF DEVICE

Table 3.26. (cont'd).

MEG.	ADJ.	UOLTAGE		REGULATORS-LM137K;		TEMPERATURE:	125	DEG C ;	30	APR	79
PAKAML TE	TEN COMBIT	DIT: AN	LO-LIMIT	1. 8.8	8 N/S	G . 2.5	MI-LIMIT UNITS	T UNITS			
00011 000112 000112	4444 4444 14444		9999 9999 MMMM				*****	>>>>			
URLINE	-4.25	'n	-23.004	-2.262M	-2.262H	-1.923M	23.00M	5			
URLOADI			-12.00m	7.3S2M	7.3528	7.917Ħ	12.00H	3			
URLOADE	2 -41.25		-12.00H	226.30	226.30	1.1318	12.00M	>			
URTH -14	-14.60 PLIED FOR	1500 1500 R 10.5Hsec.)	-5. 006H	1.583ff	1.583H	1.584M	5. 000 H	ɔ			
IADUI	-4.25	v	25.00U	71.830	71.830	72.420	100.0∪	•			
18012	-41.25	v	25.00U	74.79U	74.790	75.170	196.90	٩			
170610		•	1-5.000U	2.9640	2.9640	2.7500	2.000∪	₫			
DIADJ2 (LOAD		5	-5.000U	-311. 0 N	-311. 0 N	-254.5N	2.000	₫			
COOUT COOUT FREAK COUT	1051 -4.25 (VOUT) RECOV. 1052 -40.32 (VOUT) RECOV. IPERK -4.25 (VOUT) RECOV.	υξ +Άι ∪ Γ • Θυ υΓ•-1.9υ	1	4.4.5.5.5.5.5.5.5.5.5.5.5.5.5.5.5.5.5.5		21.12.11.12.12.12.12.12.12.12.12.12.12.1		<i>«»«»«»</i>			
IO1 IO2 IO3 USTART	-14.25 -11.25 -41.25	UF1.40 UF1.40 UF1.40	1	508.00 508.00 1.760H	448.9U 508.9U 1.769H	456.eU 516.eU 1.696H -1.244	MUN 1-				
NEG.	ADJ.	VOLTAGE	REGULATO	REGULATORS-LM137K	•	TEMPERATURE:	150	DEG C ;	30	APR	79
PARAMETER		=	LO-LIMIT	5/H	8 N/S	8 N S	HI-LIMIT UNITS	UNITS			
VOUTS	200 200 200 200 200 200 200 200 200 200	17. (#9) 18. (#9)	-1.300	-1.362	-1.252	-1.252	1-1.200	3			

TABLE 3.27. NEG. ADJ. VOLTAGE REGULATOR - LM137K $T_{A} = 25^{\circ}$ C

6-12-79

PARAMETER	CONDITIONS	LO - LIMIT	S/N7	S/N8	6N/S			HI - LIMIT	UNITS
△ V _{IN} △ V _{OUT}	$v_{IN} = -6.25v$ $e_i = 1 v_{RMS}$ $e_i = 2.400 v_{IS}$ $e_i = 1 v_{RMS}$ $e_i = 1 v_{RMS}$ $e_i = 1 v_{RMS}$ $e_i = 1 v_{RMS}$	50	59.2	58.4	6.09	1	t.	1	æ
V _{NO}	v_{IN} = -6.25V I_{L} = 100 mA	ı	70	70	70	1	•	120	uV RMS
△ V _{OUT} △ V _{IN}	$V_{IN} = -6.25V.$ $\Delta V_{IN} = -1.0 V$ $I_L = 10 mA$	-	30	32	30			640	mV/V
A VOUT	$V_{\text{IL}} = -6.25V$ $I_{\text{L}}^{\text{IN}} = 100 \text{ mA}$ $\triangle I_{\text{L}} = 400 \text{ mA}$	-	50°	.063	•045	ı	•	0.15	mV/mA

6-15-79 (cont'd). $T_A = 25^{\circ}C$ Table 3.27. NEG. ADJ. VOLTAGE REGULATOR - LM137K

1-1	· - 1	1		
UNITS	ф	uVRMS	mV/V	mV/mA
HI - LIMIT	ŧ	120	70	0.15
S/N6	59.2	70	38	20°
S/NS	58.8 59.2	70	35	\$0.
S/N4	58.8	70	34	•045
S/N2	60.9	70	30	•05
S/N1 S/N2	6.09	70	30	.045
TO - LIMIT	20	•	ı	
CONDITIONS	$V_{IN} = -6.25V$ $Q_{i} = 1 V_{rms}$ $Q_{i} = 2400 Hz$ $I_{L} = 500 mA$	VIN = -6.25V IL = 100 mA	$V_{IN} = -6.25V$ $\Delta V_{IN} = -1.0 V$ $I_L = 10 \text{ mA}$	$V_{IN} = -6.25V$ $I_L = 100 \text{ mA}$ $\Delta I_L = 400 \text{ mA}$
PARAMETER	△ V _{IN}	V _{NO}	△ V _{OUT} △ V _{IN}	△ V _{OUT}

Table 3.28. Comparison of 3-Terminal Device Data (25°C)

	Condi	tion					1
Parameter	V _{IN} (V)	I2 (mA)	LM117H	LM117K	LM137H	LM137K	Units
V _{OUT 1}	4.25	5	+1.240	+1.246	-1.252	-1.255	v
V _{OUT 2}	4.25	IMAX	+1.233	+1.245	-1.245	-1.250	. V
VOUT3	41.25	-MAX 5	+1.247	+1.251	-1.255	-1.257	V
VOUT4	41.25	11	+1.245	+1.248	-1.254	-1.257	v
V _{RLINE}	4.25 } 41.25 }	5,	+5.771	+4.235	-2.477	-2.418	. mV
V _R LOAD1	6.25	5 }	-5.237	050	+11.39	+4.722	mV
V _{RLOAD2}	41.25	IMAX S	-1.663	-2.174	+1.041	+ .749	mV
V _{RTH}	41.25 14.60	I ₂ I ₃	+2.941	+3.142	+ .430	+1.032	Vm Vm
I _{ADJ} 1	4.25	5	-50.11	-55.761	+68.64	+66.78	l uA
(LINE) I _{ADJ} 2 (LINE)	41.25	5	-50.74	-56.127	+71.67	+69.78	ı uA
(LINE) (LINE)	4.257	5	635	365	+3.026	+3.003	, uA
△ Ì _{ADJ} (LOAD)	6.25	5 IMAX	682	155	-1.090	519	uA
<u> </u>	. 05	-0	1 0/0			1	
Ios1	4.25	v _{out} =0v	-1.240	-2.711	+1.216	+2.294	, A
VOUT RECOV	40.00	-0	+1.236	+1.247	-1.241	-1.250	V
IOS2	40.00	v _{our} =0v	226	471	+ .340	+ .614	A
VOUT RECOV	4.25	lasz1 _ 1 Ozz	+1.249		-1.254	-1.257	V :
I _{PEAK} V _{OUT} RECOV	4.25	△ V _{OUT} =-1.0V	+1.236	-2.409 +1.247	+1.221	+2.340	, A , V;
101	4.25	1v _{OUT} ; =1.4v	-1.293	-1.318	+ .408	+ .414	mA
IQ2	14.25		-1.443	-1.670	+ .478	+ .554	mA.
IQ3	41.25	V _{OUT} =1.4V	-3.487	-3.729	+1.913	+2.034	mA
V _{START}	4.25	I _{MAX}	+1.234	+1.246	-1.241	-1.250	V :
I _{MAX} =			-500	-1500	+500	+1500	mA.
I ₁ =			- 50	- 200	+ 50	+ 250	mA.
I ₂ =			-125	- 500	-		mA.
I ₃ =			-	•	+750	+1500.	mA

Table 3.29. Comparison of 3-Terminal Device Data (-55°C)

	Cor	ndition	<u> </u>	<u> </u>	l	T	
Parameter	VIN (V)	II (mA)	LMl17H	LM117K	LM137H	LM137K	Units
Vout 1	4.25	5	+1.240	+1.246	-1.253	-1.252	i v
VOUT 2	4.25	IMAX	+1.234	+1.245	-1.244	-1.248	v
VOUT3	41.25	-MAX	+1.245	+1.249	-1.256	-1.255	ΙV
VOUT4	41.25	11	+1.244	+1.247	-1.256	-1.255	v
V 0014	71.23	11	71.244	1 14.24/	1.250	-1.233	; *
V _{RLINE}	4.25 }	5	+4.830	+3.192	-3.846	-3.620	mV
V _{RLOAD1}	6.25	5 }	+ .328	+ .842	+8.642	+3.195	mV
V _{RLOAD2}	41.25	5 7 I ₁	927	+ .943	+ .927	+ .537	mV
VRTH	41.25	I ₂	+4.083	+3.657	l 		mV
	14.60	13		<u> </u>	124	+ .057	mV
I _{ADJ} 1 (LINE)	4.25	5	-40.57	-46.51	+74.10	+70.97	uA
I _{ADJ2} (LINE)	41.25	5	-42.30	-46.76	+77.31	+74.36	uA
ΔI _{ADJ} (LINE)	4.25	5	-1,729	249	+3.200	+3.381	uA
∆I _{ADJ} (LOAD)	6.25	5 IMAX	-1.435	382	-1.568	832	uA.
I _{OS} 1	4.25	V _{OUT} =0v	-1,258	-2.751	+1.192	+2.241	A
VOUT RECOV		001	+1.238	+1.246	-1.244	-1.248	v
I _{OS} 2	40.00	v _{out} =ov	329	698	+ .387	+ .736	A
VOUT RECOV		001	+1,248	+1.249	-1.256	-1.255	v
IPEAK	4.25	V _{OUT} 1.0v	-1,262	-2.315	+1.202	+2.192	Å
VOUT RECOV		0011	+1,237	+1.245	-1.244	-1.248	v
		,				1	
IQ1	4.25	V _{OUT} =1.4V	-1.023	-1.052	+ .315	+ .334	mΑ
IQ2	14.25	VOUT = 1.4V	-1.380	-1.461	+ .410	+ .486	mA.
IQ3	41.25	V _{OUT} =1.4v	-3.377	-3.632	+1.964	+2.107	Am
V _{START}	4.25	I _{MAX}	+1,235	+1.245	-1.244	-1.248	v
I _{MAX} =			-500	-1500	+500	+1500	mA
I ₁ =			- 50	- 200	+ 50	+ 200	mA
I ₂ =		1	-125	- 500	-	_	mA
I3 =		ì	-	-	+750	+1500	mA
L <u></u>						 	1

Table 3.30. Comparison of 3-Terminal Device Data (125°C)

	Cond	ition				 	
Parameter	V _{IN} (V)	1 ₂ (mA)	LM117H	LM117K	LM137H	LM137K	Units
V _{OUT} 1	4.25	5	+1.235	+1.238	-1.254	-1.256	v
Vour2	4.25	IMAX	+1.225	+1.235	-1.240	-1.249	v
V _{OUT} 3	41.25	5	+1.242	+1.243	-1.256	-1.257	V
V _{OUT} 4	41.25	11	+1.240	+1.239	-1.255	-1.257	V
VRLINE	4.25	5	+7.250	+5.077	-1.946	-2.177	mV
V _{RLOAD1}	6.25	5 7	-5.101	-1.269	+15.09	+7.182	mV
V _{RLOAD2}	41.25	IMAX S	-2.500	-3.519	+1.595	+ .905	mV
VRTH	41.25	12	+2.104	+2.702			mV
•	14.60	13			+ .882	+1.484	mV
IADJ1 (LINE)	4.25	5	-55.36	-60.63	+74.00	+70.65	uA
I _{ADJ2}	41.25	5	-55.95	-61.03	+76.84	+73.50	uA
(LINE) Δ^{I}_{ADJ} (LINE)	4.25	5	585	408	+2.846	+2.852	uА
△I _{ADJ} (LOAD)	6.25	5 IMAX	235	+ .022	581	295	uA
I _{OS} 1	4.25	V _{OUT} =0v	-1.187	-2.354	+1.195	+2.170	A
VOUT RECOV	[001	+1.228	+1.237	-1.240	-1.249	V
Ios 2	40.00	v _{out} =ov	235	431	+ .318	+ .563	
VOUT RECOV	ļ	001	+1.244	+1.243	-1.256	-1.257	V
IPEAK	4.25	A V _{OUT} =-1.0v	-1.186	-1.990	+1.196	+2.104	A
V _{OUT} RECOV		- 00H	+1.227	+1.236	-1.240	-1.249	V
101	4.25	V _{OUT} =1.4v	-1.450	-1.478	+ .474	+ .455	mA
IQ2	14.25	Vour = 1.4V	-1.714	-1.771	+ .521	+ .559	mA.
IQ3	41.25	V _{OUT} =1.4V	-3.396	-3.591	+1.805	+1.818	mA
VSTART	4.25	I _{MAX}	+1.225	+1.236	-1.240	-1.249	v
I _{MAX} =			-500	-1500	+500	+1500	mA
I ₁ =			- 50	- 200	+ 50	+ 200	mA.
12 =			-125	- 500	.750	.1500	mA.
13 =				-	+750	+1500	mA

Table 3.31. Electrical performance characteristics for device type 01 (78MG)
(See 3.4 unless otherwise specified)

	1	Condition: (F	ig. 12 unless o	thomaico	,		
Characteristic	Symbol		ated)	ruerwise	1 ,,,	nits	1
CHATACCELISCIC	J J III DO I	Input Voltage		Other			Units
Output Voltage	Voim	VIN= 8V	IL=-5mA,-500mA			5.25	OUTES
Oucput Voicage	Voul	VIN=30V	IL=-5mA,-50 mA	2/	4.75	13.23	"
!		VIN=10V	IL=-5mA	TA=150°C 1/	1	ļ	!
	1	VIN=38V	I _L =-500mA	$R_1=24.9K \Omega$	20 6	31.5	{
		A TW-20A	II~Joona	R ₂ = 4.99KΩ	20.5	31.5	i l
Line regula-	VDI TNE	8V≰VIN 30V	IL=- 50mA	Figure 12	-150	150	mV
tion	VALINE	8V≤VIN 25V	IL=-350mA	Waveform	- 50		v
Load regula-	VELOAD	VIN= 10V	-500mA≤IL≤-5mA		-100		•
tion	, KLOND	$V_{IN} = 30V$	- 50mA = 1 = 5mA	Waveform	-150		
Thermal regu-	VRTH.	V _{IN} = 15V	I _{I.} =-500mA	TA=25°C	- 50		
lation	· KIII.	V 114 - 23 ·	II. Soomii	Figure 12	50	"	
1.	Ì			Waveform	1	ļ	i i
Standby cur-	ISCD	V _{IN} = 10V	I _{1.} =-5mA		-7.0	-0.5	mA
rent drain	300	VIN= 30V	I _L =-5mA			-0.5	
Standby cur-	A Iccn	8V≤V IN≤30V	I _{T.} =-5mA		-1.0		•
rent drain	(Line)	- 114			~ "		
change versus	` '				ł	1	
line voltage				•	ļ		
Standby cur-	A ISCD	$v_{IN} = 10v$	-500mA≤I _L ≤-5mA		-0.5	0.5	
rent drain	(Load)		.		1		•
change versus					l	1	1
load current					ļ	ł	į į
Control pin	ICTL	$V_{IN} = 10V$	I _I =-350mA	T _A =25°C	-5.0	-0.01	μA
current	""	•	~	-55°C ≰ T _A ≤	-8.0	-0.01	MΑ
				125°C	<u> </u>		
Output short	IOS1	V _{IN} = 10V		Figure 12	-2.0	-0.01	A
circuit cur-	I _{OS2}	$V_{IN} = 30V$		Waveforms		-0.01	
rent					<u> </u>		
Output volt-				2/	•		1
age recovery	VOUT	V _{IN} = 10V	RL=10Д;CL=20ДF	After Iosi	4.75	5.25	l v
after output	(RECOV)	$V_{IN} = 30V$	RL=IKA	After Ios2	1	l	
short circuit	1	,				1]
current	ļ			L	 		
Voltage start-	VSTART	V _{IN} = 20V	RL=10.0;CL=20цF		4.75	5.25	
up	 				 	 	
Ripple rejec-		$v_{IN} = 10v$	IL=-125mA	Figure 13	45		dB
tion	AVOUT	Ci = 1Vrms		TA=25°C]	l	}
<u></u>		@ f= 2400 Hz			₩	 	
Output noise	1]		
voltage	VNO	v _{IN} = 10v	IL=-50mA	Figure 14		125	ųV _{rms}
į	1			TA=25°C	1		
1	1 .			BW=10Hz to	1	ļ	}
7/	4 17	U	7 = 64	10kHz	├ -	1 20	
Line trans-	≜ Vout	V _{IN} = 10V	IL=-5mA	Figure 15		30	mV/V
ient response	△VIN	VPULSE=3.0V		T _A =25°C	 	<u> </u>	
Load trans-	△V OUT	VIN= 10V	IL=-50mA	Figure 16		2.5	mV/maA
ient response	AIL		∆ I _L =-200mA	TA≖25°C	Ì	!	}
'	<u> </u>	L	111-100		.	<u> </u>	L

Table 3.31. (Cont'd)

NOTES: 1. All tests performed at $T_A=125\,^{\circ}\text{C}$ may, at the manufacturer's option, be performed at $T_A=150\,^{\circ}\text{C}$. Specifications for $T_A=125\,^{\circ}\text{C}$ shall then apply at $T_A=150\,^{\circ}\text{C}$.

- 2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.
- 3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.32. Electrical performance characteristics for device type 02 (78G) (See 3.4 unless otherwise specified)

ı — — — — — — — — — — — — — — — — — — —		Condition: (Fi	ig. 12 unless ot	hamilea	T		
Characteristic	Symbol		ated)	HETATSE	1 , ,,	mits	
O.G. C.	Symbol	Input Voltage		Other		Max.	Undto
Output Voltage	Voum	V _{IN} = 8V	I _{I.} =-5mA,-1000mA			5.25	V
output vortage	VOUT	V _{IN} =30V	IL=-5mA,-100 mA		4.73	3.23	V
	1		IL=-5mA	TA=150°C 1/			
		V _{IN} =10V	IL=-1000mA		20 5	21 6	
		VIN=38V		R1=24.9K A R2=4.99K A	20.5	31.5	
Line regula-	VRLINE	8V≤V _{IN} ≤30V	IL=-100mA	Figure 12	-150	150	mV
tion		8V≤V IN €25V	IL=-500mA	Waveforms	- 50	50	
Load regula-	VRLOAD	v _{IN} =10v	-1000mA=IL≤-5m4	Figure 12	-100	100	1
tion	*******	VIN=30V	-100mA4IL4-5mA	Waveforms	-150	150	
Thermal regu-	VRTH.	V _{IN} =15V	IL=-1000mA	TA=25°C	- 50	50	
lation				Figure 12	}		
				Waveforms	i	1	· '
Standby cur-	I _{SCD}	V _{IN} =10V	IL=-5mA		-7.0	-0.5	mA
rent drain	-300	V _{IN} =30V	IL=-5mA			-0.5	
Standby cur-	△ISCD	8V4VIN430V	I _{T.} =-5mA		-1.0		1
rent drain	(LINE)	O. Z. IN Z.	~L		1	*	
change versus	(51115)						l
line voltage				ĺ			
	△ I _{SCD}	V _{IN} =10V	-1000mA = II = -5mA		-0.5	0.5	1
rent drain	(LOAD)	A IM TO A	-1000000-172-700		1-0.5	0.5	1
change versus	(FOWD)			1			l
load current			ļ	\	}		1
Control pin	7	77	I _L =~500mA	m =2500		ا م م ،	
•	^I CTL	V _{IN} =10V	TL200mA	T _A =25°C		-0.01	
current				-55 C=TA	-8.0	-0.01	LAA.
Output shows	Tool	··		125°C	1.0	0.00	
Output short	Ios1	V _{IN} =10V		Figure 12		-0.02	
circuit cur-	Ios2	$\Lambda^{IN}=30\Lambda$		Waveforms	-2.0	-0.02	1
rent	 			ļ <u>.</u>			ļ <u>.</u>
Output voltage		V _{IN} =10V	RL=5.12; CL=20µF	After Iosi	4.75	5.25	V
recovery after	(RECOV)	l.		2/	1	j	
output short					ţ	1	J
circuit cur-		VIN=30V	$R_L = 1 K \mathcal{A}$	After Ios2	1]
rent							1
Voltage start-	VSTART	VIN =20V	RL=512;CL=20uF		4.75	5.25	
up		L		<u> </u>			
Ripple rejec-	AVIN	V _{IN} =10V	I _L =-350mA	Figure 13	45		d B
tion	AVOUT	Ci=1Vrms		T _A =25°C	i		Į
		@ ₹= 2400 Hz	Ì	~		i	
Output noise	V _{NO}	V _{IN} =10V	IL=-100mA	Figure 14		250	µV _{rms}
voltage				TA=25°C	l	1	Line
				BW=10 Hz to		l	ł
		}		10kHz	ļ		1
Line trans-	△ V _{OUT}	V _{IN} =10V	I _{I.} =-5mA	Figure 15		30	mV/V
ient response		VPULSE=3.0V		TA=25°C		رد ا	mv / v
response	AVIN	. LOTOE-2.0A	<u> </u>	IA 23 C		<u></u>	<u> </u>
lood trans-	AVar	V=10V	T- =-100-4	Figure 16			
Load trans-	AVOUT	V _{IN} =10V		Figure 16	1	۔ ا	l
ient response	AIL	<u> </u>	III-101	T _A =25°C		2.5	mV/mA

Table 3.32. (Cont'd)

- NOTES: 1. All tests performed at $T_A=125\,^{\circ}\text{C}$ may, at the manufacturer's option, be performed at $T_A=150\,^{\circ}\text{C}$. Specifications for $T_A=125\,^{\circ}\text{C}$ shall then apply at $T_A=150\,^{\circ}\text{C}$.
 - Output voltage recovery test shall be performed, with the designed load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.
 - 3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.33. Electrical performance characteristics for device type 03 (LM117H) (See 3.4 unless otherwise specified

	ſ	Condition: (F	ig. 12 unless o	therwise	l		
Characteristic	Symbol	1	ated)		Li	mits	
		Input Voltage	Load Current	Other	Min.	Max.	Unita
Output Voltage	VOUT	V _{IN} =4.25V	IL=-5mA,-500mA	3/	1.200	1.300	V
	Ì	V _{IN} =41.25V	IL=-5mA,- 50mA	_	Ì		
	<u> </u>	VIN=6.25V	IL=-5mA	TA=150°C 1/			
Line regula-	VRLINE	4.25V≤V _{IN}	I _L =-5mA	TA=25°C	- 9	9	mV
tion		≤ 41.25V		-55°C≰TA	-23	23	
	<u> </u>			≤ 125°C			
Load regula-	VRLOAD	v _{IN} =6.25V	-500mA = I _ = -5mA	T _A =25°C	-3.5		-
tion	l		_	-55°C TA	-12	12	
				₹125°C	L	L	
		V _{IN} =41.25V	-50mA = IL = -5mA	T _A =25°C	-3.5		
	Ì			-55°C ≈ TA	-12	12	
 	<u> </u>	ļ		- 125°C		ļ	
Thermal regu-	VRTH.	V _{IN} =14.6V	IL=-750mA	TA=25°C	- 5	5	
lation	<u> </u>						
Adjust pin	IADJ	V _{IN} =4.25V	IL=-5mA		-100	1	μA
current	<u></u>	VIN=41.25V	IL=-5mA			-15	
Adjust pin	△ IADJ	4.25V\$IL	IL=-5mA		- 5	5	
current change	(LINE)	≨ 41.25V		ł	ł	ł	}
versus line					l		
voltage	A -		500 185 8 5			 	1
Adjust pin	IADJ	V _{IN} =6.25V	-500mA = IL = -5mA		- 5	5	
current change	(LUAD)		ļ	}]		
versus load			-	•	ĺ	i	i
current	T.	4.25V ≤ VIN			2 00	-0.50	
Minimum load	IQ	4.25V IN ≤ 14.25V forced			-3.00	-0.30	πA
current		VOUT=1.4V				İ	ĺ
		$V_{IN} = 41.25V$			 	 -	ł
		forced Vour		ļ	Ls 00	-1.00	mA
	i i	=1.4V			[3.00	[1.00	HILES.
Output short	I _{OS} 1	VIN=4.25V		 	-1.8	-0 5	A
circuit cur-	IOS 2	V _{IN} =40V		· · · · · · · · · · · · · · · · · · ·		-0.05	Ā
rent	-032	, TM			``.	1 5.55	^
Output volt-	VOUT	VIN=4.25V	R _L =2.5 .0 ; C _L =20µF	After Toos	1.200	1.300	V
tage recovery		V _{IN} =40V	RL 23031	27	[Γ.,	1
after output	\	- 414		After IOS2		l	l
short circuit	Ì					ł	1
current				ļ		1	
Voltage start-	VSTART	V _{IN} =4.25V	R _L =2.5/1;C _L =20 _µ F		1,200	1.300	1
up	DIAM			Į			
Ripple rejec-	AV IN	VIN=6.25V	IL=-125mA	Figure 13	65		dB
tion		Ci=1Vrms		TA=25°C		ļ	1
	VUIT	@fo=2400 Hz				ł	1
Output noise	V _{NO}		I=-50mA	Figure 14		120	µVrms
voltage	,,,		_ =	TA=25°C		- /-	
_				BW=10Hz to		!	i
	'			10kHZ			1
							L
			III-102				

Table 3.33. Electrical performance characteristics for device type 03 (LM117H) (Cont'd) (See 3.4 unless otherwise specified

	<u> </u>	Condition: (ig. 12 unless	otherwise	T		
Characteristic	Symbol	st	ated)		Li	mits	
		Input Voltage	Load Current	Other	Min.	Max.	Units
	△VOUT	V _{IN} =6.25V V _{IN} =3.0V	IL=-10mA	Figure 15 T _A =25°C		6	mV/V
	▲VIN	V _{IN} =6.25V	IL=-50mA A I _L =-200mA	Figure 16 T _A =25°C		0.6	mV/mA

- NOTES: 1. All tests performed at $T_A=125\,^{\circ}\text{C}$ may, at the manufacturer's option, be performed at $T_A=150\,^{\circ}\text{C}$. Specifications for $T_A=125\,^{\circ}\text{C}$ shall then apply at $T_A=150\,^{\circ}\text{C}$.
 - 2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.
 - 3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

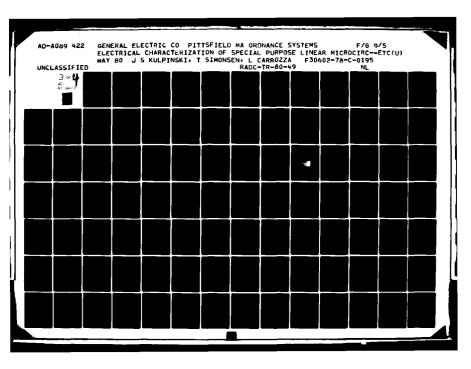


Table 3.34. Electrical performance characteristics for device type 04 (LM117K) (See 3.4 unless otherwise specified)

Characteristic						mits	
			Load Current	Other			Units
Output Voltage	Vour	VIN=4.25V	IL=-5mA,-1500mA	<u>3</u> /	1.200	1.300	V
		VIN=41.25V	IL=-5mA,-200mA	_	1		
		V _{IN} =6.25V	IL=-5mA	TA=150°C 1/	1		
Line regula-	VRLINE	4.25€IL	IL=-5mA	TA=25°C	-9	9	mV
tion		≰41.25 V		-55°C⊈TA	-23	23	
			<u> </u>	≤ 125°C			!
Load regula-	VRLOAD	V _{IN} =6.25V	-1500mA = IL = 5mA		-3.5	3.5	
tion				-55°C €TA	-12	12	
			<u> </u>	≤ 125°C			
		VIN=41.25V	-150mA=IL=-5mA	TA=25°C	-3.5	3.5	
				-55°C-TA	-12	12	•
				≤ 125°C			
Thermal regu- lation	VRTH.	V _{IN} =14.6V	I _L =-1500mA	T _A =25°C	-5	5	
Adjust pin	IADJ	V _{IN} =4.25V	IL=-5mA		-100	-15	Aιζ
current	,,,,,	V _{IN} =41.25V	I _L =-5mA		-100		
Adjust pin	4 [ADJ	4.25V4VIN	IL=-5mA		-5	5	
current		≤ 41.25V	_			_	
change versus	,						
line voltage							
Adjust pin	4 IADJ	V _{IN} =6.25V	-1500mA = IL <-5mA		-5	5	
current	(LOAD)						
change versus		į		ĺ	<u> </u>		1
load current				ļ	f i		1
Minimum load	I_Q	4.25V≰IL			-3.00	-0.50	mA
current	`	≤ 14.25V					ĺ
		forced Vour]
		=1.4V		1			1
		V _{IN} =41.25V			-5.00	-1.00	mA
		forced Vour					• • •
		=1.4V					
Output short	Ios1	VIN=4.25V			-3.50	-1.50	A
circuit cur-	IOS 2	V _{IN} -40V			-1.00	-0.18	A
rent		_		, .			
Output volt-	Vout	V _{IN} =4.25V	RL=.8334;CL=20µF	After IOS1	1.200	1.300	v
age recovery	(RECOV)	VIN=40V	R _L =250.2	2/			1
after output				After IoS2	1		1
short circuit							
current							l
Voltage start-	VSTART	V _{IN} =4.25V	$R_L = .8330; C_L = 20 \mu F$		1.200	1.300	
up]			l		<u> </u>
Ripple rejec-	4V _{IN}	V _{IN} =6.25V		Figure 13			
tion	AVOUT	Ci=1Vrms @fo=2400 Hz	IL=-500mA	TA=25°C	65		dB
Output noise	v _{NO}	V _{IN} =6.25V	IL=-100mA	Figure 14			
voltage	,,,,			TA=25°C	[1
_				BW=10Hz to		120	uVrms
				10kHz			_

Table 3.34. Electrical performance characteristics for device type 04 (LM117K) (See 3.4 unless otherwise specified)

Characteristic	Symbol	st.	ig. 12 unless (ated)	otherwise.	Li	mits	
Y 4 a - b		Input Voltage	Load Current	Other			Unite
		V _{IN} =6.25V A V _{IN} =1.0V	IL=-10mA	Figure 15 TA=25°C		6	mV/V
Load trans- ient response	VOUT	V _{IN} =6.25V	IL=-100mA AI L=-400mA	Figure 16 TA=25°C	~-	0.30	mV/mA

- NOTES: 1. All tests performed at TA=125°C may, at the manufacturer's option, be performed at TA=150°C. Specifications for TA=125°C shall then apply at TA=150°C.
 - Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.
 - 3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.35. Electrical performance characteristics for device type 01 (79MG)

(See 3.4 unless otherwise specified)

Characteristic		·	ig. 12 unless	otherwise	1.4	mits	
Characteristic	Symbol	Input Voltage	Load Current	Other		Max.	Units
Output Voltage	Vorm	VIN=-8V	IL=5mA,500mA			-4.75	V
odeput vortage	4001	V _{IN} =-30V	IL=5mA,50mA	2/	1 7:-1	4.,5	•
		VIN=-10A		TA=150°C 1/	j		
	•	VIN=-38V		R1=27.4ka	-21 6	-28.5	
		 A TM_=20A		R2=2.21k.0	-31.3	-20.5	
Line regula-	VRLINE	-30V4V IN -8V		Figure 12	-150	150	mV
tion	MULINA	-25V4VIN4-8V		Waveforms	- 50	50	
Load regula-	VRLOAD	VIN=-10V	5mA4IL4500mA		-100		
tion	· KLOAD	VIN=-30V	5mA ≤IL ≤50mA		-150		
Thermal regu-	VRTH.	V _{IN} =-15V		TA-25°C	- 50	50	
lation	'KIR.	, TM 724		Figure 12			
1001011				Waveforms			
Standby cur-	ISCD	V _{IN} =-10V	IL=5mA	Mayerormo	0.1	3.0	mA
rent drain	TSCD		1		0.1	4.0	
	A T = = -	V _{IN} =-30V -30V = V _{IN} =-8V	IL=5mA		-1.0	1.0	
Standby cur-	△ISCD	-2007 NIV01	I _L =5mA		1-1.0	1.0	
rent drain	(LINE)		\		1		
change versus					1 1		1
line voltage			7-7-7-7-7		 		
Standby cur-		V _{IN} =-10V	5mA 41L 4500mA		-0.5	0.5]
rent drain	(LOAD)				i i		Ì
change versus					1 1		ļ
load current			<u> </u>	·			<u> </u>
Control pin	ICTL	V _{IN} =-10V	IL=350mA	TA=25°C	0.001		JLΑ
current)	}		-55°C4TA	0.001	3.00	AU,
<u> </u>	L			=125°C	1		
Output short	Ios 1	V _{IN} =-10V		Figure 12	0.002	2.0	A
circuit cur-	IOS 2	V _{TN} =-30V	1	Waveforms	0.002	1.0	1
rent		1			·		L
Output voltage	VOUT	VIN=-10V	RL=10A;CL	After IOS1	-5.25	-4.7	v
recovery after			=20µ£	2/	1	l	1
output short	,	VIN=-30V		After 1082	}	1 .	1
circuit cur-	l						1
rent	Ì]	,			l	1
Voltage Start-	VCTADT	V TN=-20V	RL=10a;CL		-5.25	-4.7	
up	ASTURE	I IN 201	=20µF	ł	1	1	1
Ripple rejec-	4VIN	V _{IN} =-10V	I _L =125mA	Figure 13	45		dB
kipple lejec- tion		C _i =1Vrms	I'l reams	TA=25°C	75		ا س
Lion	AVOUT		Ì	1A 23 C	}	1	1
0	17	@f=2400 Hz	T- =50-4	Pious 14	 	200	wr
Output noise	VNO	V _{IN} =-10V	IL=50mA	Figure 14		23	י איין י
voltage	[l	TA=25°C	[l	
	}	1		BW=10Hz to	1	ĺ	1
Line trans-	△VOUT	V _{IN} =-10V	I _L =5mA	10kHz Figure 15	 -	30) <u>=v</u> /
ient response			~L Junes	TA=25°C	1	~	1-"
	AVIN	VPULSE=-3.0V	1 _L =50mA	Figure 16	+	 	+
Load trans-	AVOUT	V _{IN} =-10V	1L-30mA	TA=25°C	l		5 mV/
ient response	AIL	1	♣1L-200mA	TA-43 C	1	4.	7 WY/

Table 3.35. (Cont'd)

NOTES: 1. All tests performed at TA=125°C may, at the manufacturer's option, be performed at TA=150°C. Specifications for TA=125°C shall then apply at TA-150°C.

- 2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.
- 3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.36. Electrical performance characteristics for device type 02 (79G)
(See 3.4 unless otherwise specified)

Ch	Complete		Fig. 12 unless	otherwise			
Characteristic	Symbol		tated)	T 0.1		mits	
0		Input Voltage				Max.	Units
Output Voltage	VOUT	VIN=-8V	IL=5ma,1000mA	<u>3</u> /	-5.25	-4.75	V
		V _{IN} =-30V	IL=5mA,100mA		}		
	1	VIN=-10V		TA=150°C 1/			
		VIN=-38V	I =1000mA	R1=27.4k .1 R2=2.21k .1		-28.5	
Line regula-	VRLINE	-30V4VIN -8V	IL=100mA	Figure 12	-150		mV
tion		-25V±VIN±-8V	II_= 500mA	Waveforms	- 75	75]
Load regula-	VRLOAD	V _{IN} =-10V	5mA = I L=1000mA	Figure 12	-100	100	i i
tion		VIN=-30V	5mA≤IL≤100mA	Waveforms	-150	150	ļ
Thermal regu-	VRTH.	V _{IN} =-15V	IL=1000mA	TA=25°C	- 50	50	!
lation				Figure 12)		
				Waveforms	}		Í
Standby cur-	ISCD	V _{IN} =-10V	IL=5mA		0.5	3.0	mA
rent drain	-300	VIN=-30V	IL=5mA		0.5	i 1	
Standby cur-	△ISCD	-30V±VIN ±-8V	IL=5mA		-1.0		
rent drain	(LINE)	30121112 OV	I Dawn			2.0	!
change versus	(DINE)		•	{		ļ	į
line voltage				į	[,
Standby cur-	A TOOR	VIN=-10V	5mA = II = 1000mA		-0.5	0.5	,
rent drain	4 ISCD	VIN10V	DIMATIC TOOONIA		-0.3	0.5	
	(LOAD)				·		
change versus	ļ	•				!	;
load current			\	2.20			<u> </u>
Control pin	ICTL	V _{IN} =-10V	IL=500mA	T _A =25°C		2.00	
current	ļ				0.001	3.00	Aμ
	l			£ 125°C	<u> </u>		
Output short	Ios1	V _{IN} =-10V			0.002		A
circuit cur-	IOS2	VIN=-30V	1	Waveform	0.002	2.0	
rent					İ		
Output voltage	VOUT	VIN=-10V	R _{I.} =5. α ;C _{I.} =20μF	After Ios1 2/	-5.25	-4.75	V
recovery after		V _{IN} =-30V		After IOS2			
output short	1			1	ļ	j	1
circuit cur-						j '	
rent				Ì	1)	
Voltage start-	VCTADT	VINE-20V	RL=5.0;CL=20uF		-5 25	-4.75	1
up	VSTART	ATM -FOA	WE DESCRIPTION	Ì	-3.23	7.73	1
Ripple rejec-	△ V IN	V _{IN} =-10V	IL=350mA	Figure 13	45		dв
tion		C _i =1Vrms	I II - 3 30 IIM	TA=25°C	43		u b
Clon	AVOUT			1A-23 C			1
0.5		@f=2400Hz	= 100	m · 1/		350	-
Output noise	VNO	VIN=-10V	I _L =100mA	Figure 14		250	µVrms
voltage	,			TA=25°C			
				BW=10Hz to			
	L			10kHz			
Line trans-	AVOUT	V _{IN} =-10V	IL=5mA	Figure 15		30	mV/V
ient response	4V IN	VPULSE=-3.0V	1	TA=25°C			L
Load trans-	∆ VOUT	V _{IN} =-10V	I _L =100mA	Figure 16		2.5	mV/mA
ient response	AIL	_ ,	△ IL=400mA	TA=25°C			l

Table 3.36. (Cont'd)

NOTES: 1. All tests performed at $T_A=125\,^{\circ}\text{C}$ may, at the manufacturer's option, be performed at $T_A=150\,^{\circ}\text{C}$. Specifications for $T_A=125\,^{\circ}\text{C}$ shall then apply at $T_A=150\,^{\circ}\text{C}$.

- Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output condition. Voltage recovery for conditions other than those specified is not guaranteed.
- 3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.37. Electrical performance characteristics for device type 03 (LM137H)

(See 3.4 unless otherwise specified)

Output Voltage VOUT VIN=-4.25V VIN=-4.25V VIN=-6.25V Line regula- tion VRLINE -41.25V2VIN 2-4.25V Load regula- tion VRLOAD VIN=-6.25V SmA=IL=5mA TA=150°C TA=25°C -9 9 -23 23 Load regula- tion VRLOAD VIN=-6.25V SmA=IL=500mA TA=25°C -6 6 -55°C4TA -12 12 -24 24 -125°C SmA=IL=500mA TA=25°C -12 12 -24 24 -255°C Thermal regu- lation VRTH. VIN=-41.25V SmA=IL=50mA TA=25°C -6 -55°C4TA -12 12 -24 24 -125°C VIN=-41.25V SmA=IL=50mA TA=25°C -55°C4TA -12 12 -24 24 -125°C -55°C4TA -12 12 -55°C4TA -12 -55°C4TA -12 -55°C4TA -12 -55°C4TA	Symbol	st	ated)				
		Input Voltage	Load Current	Other	Min.	Max.	Jnits
VIN=-41.25V	VOUT		IL=5mA,500mA	3/	-1.300	-1.20Q	V
VIN = -6.25V			It = 5mA . 50mA		1	1	
Line regulation				TA=150°C 1/			
Cload regulation	VOI THE			TA=25°C	-9	9	mV
125°C -6 6 -55°CdTA -12 12 12 12 12 12 12 1) LL 300.			23	
Thermal regulation		1-4.234	ļ				
Thermal regu- VRTH. VIN=-41.25V SmA±IL±500mA TA=25°C -12 12 12 12 12 12 12 1			- 14 = 4000-A				
SmA_IL_500ma	Vrload	V _{IN} =-6.25V	5mA=IL=200mA				
SmA=IL=500mA TA=25°C -12 12 24 24 2125°C -24 24 24 2125°C -24 24 24 2125°C -25°C*TA -12 24 24 25°C -25°C*TA -12 12 25°C -6 6 -55°C*TA -12 12 12 12 12 12 12 1	1	j	}	-55 C=TA	-12	12	
VIN=-41.25V 5mA fl f50mA TA=25°C -6 6 6 -55°C fTA f125°C -6 6 6 -55°C fTA f125°C -12 12 12 125°C -12 12 12 12 12 12 12 1				=125°C			
VIN=-41.25V 5mA±IL±50mA TA=25°C -6 6 -55°C±TA ±125°C -12 12 12 12 12 12 12 1			5mA_IL_500mA	TA=25°C	-12	12	
VIN=-41.25V 5mA \(\frac{1}{2}\) 50mA TA=25°C -6 6 6 -55°C \(\frac{1}{2}\) -12 12 Thermal regulation VRTH. VIN=-14.6V IL=750mA TA=25°C -5 5 Adjust pin IADJ VIN=-4.25V IL=5mA 25 100 Current Adjust pin Current Change versus Cha				-55°C≰TA	-24	24	
VIN=-41.25V 5mA \(\frac{1}{2}\) 50mA TA=25°C -6 6 6 -55°C \(\frac{1}{2}\) -12 12 Thermal regulation VRTH. VIN=-14.6V IL=750mA TA=25°C -5 5 Adjust pin IADJ VIN=-4.25V IL=5mA 25 100 Current Adjust pin Current Change versus Cha			1	125°C			
Thermal regulation Adjust pin		VTN=-41 25V	5mA STr SOmA		- 6	6	
Thermal regu- VRTH. VIN=-14.6V IL=750mA TA=25°C -5 5		ATM -4T.57A	Amera-TD-Comme				
Thermal regu- lation Adjust pin current Adjust pin current Adjust pin current Adjust pin current Adjust pin current Adjust pin current Adjust pin current Adjust pin current Adjust pin current Change versus line voltage Adjust pin current Change versus load current Change versus load current Change versus load current Minimum load current Minimum load Current Courrent Cou		j	1				
lation Adjust pin current Adjust pin current Adjust pin current Change versus line voltage Adjust pin current change versus load current Minimum load curren		-			 _		
Current Adjust pin Current C	VRTH.	V _{IN} =-14.6V	IL_ /50mA	TA=25 °C	- >	ן כ	
Current							
VIN=-41.25V IL=5mA 25 100	IADJ	VIN=-4.25V	IL=5mA	ţ			βIA
Adjust pin current change versus line voltage Adjust pin current (LOAD) VIN=-6.25V 5mA = IL = 500mA	••••	VIN=-41.25V	IL=5mA		25	100	
Current Change versus Ch	ALADI		II.=5mA		- 5	5	
change versus line voltage Adjust pin (LOAD) (LOAD	(I INE)	1 -		<u> </u>			
1 1 2 2 2 2 2 2 2 2	(DIND)	- 4.231	1		l		
Adjust pin current change versus load current Minimum load curren	ı	\	1	1	ł	}	} ·
Current change versus load current Minimum load current Minimum load current Minimum load current Minimum load current IQ			C-44T 4500-A	 	- 5	-	ł
Change versus load current Minimum load current IQ		VIN=-6.25V	DMY TIT TOOMY	· ·	1 - 3 .	{ }	1
10ad current	(LOAD)		1		}	i	ł
Minimum load current I_Q	! !	-	İ	Į.	ļ		l .
Current -4.25 V forced Vour =-1.4V VIN=41.25V forced Vour =-1.4V VIN=41.25V forced Vour =-1.4V VIN=-4.25V circuit cur- rent Output short circuit cur- rent Output voltage recovery after output short circuit cur- rent Voltage start- Voltage start- UD Ripple rejec- tion AVIN -4.25V VIN=-4.25V RL=2.5A;CL =20µF RL=2.50. RL=2.5A;CL =20µF RL=250. After Ios1 -1.300-1.200 RL=2.5A;CL =20µF RL=250. Figure 13 TA=25°C 48]	<u> </u>	<u></u>	1		.
Current -4.25V forced Vour =-1.4V VIN=41.25V forced Vour =-1.4V Output short circuit cur- rent Output voltage recovery after output short circuit cur- rent Voltage start- Voltage start- Voltage start- voltage start- voltage rejec- tion -4.25V forced Vour VIN=-4.25V forced Vour VIN=-4.25V RL=2.5a;CL =20µF RL=2.5a;CL =20µF RL=2.5a;CL =20µF Figure 13 TA=25°C 48	In	-14.25V4V _{TN}			D.20	β.00 .	mA
forced VOUT =-1.4V	- Q		1		:]	
=-1.4V	l	1		• • • •	j ·	1	1
VIN=41.25V forced VOUT =-1.4V Output short circuit cur- rent Output voltage recovery after output short circuit cur- rent Voltage start- Voltage start- up Ripple rejec- tion VIN=4.25V forced VOUT VIN=-4.25V VIN=-4.25V RL=2.5a;CL =20µF RL=2.5a;CL =20µF RL=2.5a;CL =20µF RL=2.5a;CL =20µF Figure 13 TA=25°C 48						1	· ·
Column	İ		+	1	1.00	5.00	1
=-1.4V			1	1	1	1	1
Output short circuit current Output voltage recovery after output short circuit current Voltage start- voltage start- up Ripple rejec- tion VIN=-4.25V VIN=-4.25V RL=2.5a;CL After IOS1 -1.300-1.200 RL=2.5a;CL After IOS1 -1.300-1.200 RL=2.5a;CL After IOS1 -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 RL=2.5a;CL -1.300-1.200 Ripple rejec- AVIN AVOUT Ci=1Vrms			1	1	Į.	ļ	ł
circuit cur- rent Output voltage recovery after output short circuit cur- rent VIN=-4.25V RL=2.5a;CL =20µF RL=250.a. After IOS1 2/ After IOS2 After IOS2 VIN=-4.25V RL=250.a. RL=2.5a;CL =20µF RL=250.a. Figure 13 TA=25°C 48	<u> </u>			 	h =	1 0	A
rent Output voltage recovery after output short circuit current Voltage start VSTART VIN=-4.25V RL=2.5a;CL After IOS1 -1.300-1.200 RL=250a After IOS2 RL=2.5a;CL 2/ RL=250a After IOS2 RL=2.5a;CL 2/ RL=250a Figure 13 TA=25°C 48			1				
Output voltage recovery after (RECOV) VIN=-4.25V RL=2.5.A; CL =20µF 2/RL=250.A After IOS1 -1.300-1.200 RL=250.A After IOS2 -1.300-1.200 RL=250.A After IOS2 -1.300-1.200 RL=250.A After IOS2 -1.300-1.200 RL=2.5.A; CL =20µF Ripple rejec- AVIN AVOUT Ci=1Vrms	Ios 2	V _{IN} =-40V		1	כט. ט	۲.5	A
recovery after output short circuit current Voltage start - VSTART VIN=-4.25V RL=2.5 a; CL = 20µF Ripple rejec - 4VIN AVOUT Ci=1Vrms WIN=-4.25V IL=125mA Figure 13 TA=25°C 48		<u> </u>			1 - 222	1 222	├
recovery after output short circuit cur- rent Voltage start- Up Ripple rejec- tion RECOV) VIN=-40V RL=250	VOUT	VIN=-4.25V		After Iosi	1-1.300	7~1.20 0	l v
output short circuit cur- rent Voltage start- VSTART VIN=-4.25V RL=2.5 A; CL = 20 µF Ripple rejec- AVIN AVOUT Ci=1Vrms RL=250 A After IOS2 After IOS2 -1.300-1.200 -1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200 -1.300-1.200				2/	1		}
circuit cur- rent Voltage start - VSTART VIN=-4.25V RL=2.5 A; CL = 20 µF Ripple rejec - AVIN AVOUT Ci=1Vrms RL=2.5 A; CL = -1.30C-1.200 RL=2.5 A; CL = 120 µF Figure 13 TA=25°C 48		1		After Ios2	}	1	1
rent Voltage start - VSTART VIN=-4.25V RL=2.5 a; CL = 20 µF Ripple rejec - AVIN AVOUT Ci=1Vrms RL=2.5 a; CL = 20 µF Figure 13 TA=25°C 48		1	\ _	1	1	1	1
Voltage start - V _{START} V _{IN} =-4.25V R _L =2.5 a; C _L -1.30Q-1.200	į	1	1		1	1	l
Voltage start VIN	17	17 = 4 2517	P- =2 5 0.C.	 	-1.300	-1,200	1
Ripple rejec- ΔV_{IN} $V_{IN}^{=-6.25V}$ $I_{L}^{=125mA}$ Figure 13 $I_{A}^{=25°C}$ 48	VSTART	N IN4.53A		1		٦	1
tion TA=25°C 48		 		7.	 	├ ───	
{*==**	AVIN	$V_{IN}=-6.25V$	IL=125mA	rigure 13	,,	1	dB
	AVOUT		1	TA=25°C	48]	1 "
			· l	l	1	[
·	i	1	I	<u>i</u>	<u> </u>	<u></u>	1
		VRLINE VRLOAD VRLOAD VRLOAD VRLOAD VRLOAD IADJ (LINE) AIADJ (LOAD) IQ IOS1 IOS2 VOUT (RECOV VSTART	Input Voltage	Symbol Stated Input Voltage Load Current VIN=-4.25V IL=5mA,500mA IL=5mA,500mA IL=5mA IL=25mA IL=25mA IL=125mA mbol Stated Load Current Other Vout Vin=-4.25V IL=5mA, 500mA IL=5m - 50°C IL=5mA Vin=-4.25V IL=5mA SomA IL=5m - 50°C IL=5mA IL=5m - 50°C IL=5mA IL=5m - 55°C IL=5m IL=5mA IL=5s°C IL=5mA IL=5s°C IL=5mA	Symbol Stated Lit	Symbol Stated Limits Load Current Other Min. Max. VIN=-4.25V IL=5mA, 500mA 3/1.300-1.200 VIN=-6.25V IL=5mA, 50mA TA=150°C 1/ VIN=-6.25V IL=5mA TA=25°C -9 9 -4.25V TA=150°C TA=1	

Table 3.37. Electrical performance characteristics for device type 03 (LM137H) (Cont'd) (See 3.4 unless otherwise specified)

Characteristic		1	ig. 12 unless ated)	otherwise	Li	mits	
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output noise voltage	VNO	V _{IN} ≠-6.25V		Figure 14 T _A =25°C BW=10 Hz to 10kHz		120	μVrms
Line trans- ient response		V _{IN} =-6.25V 4 V _{IN} =-1.0V		Figure 15 T _A =25°C		80	mV/V
Load trans- ient response	▲ VOUT	VIN=-6.25V		Figure 16 T _A =25°C		0.30	mV/mA

- NOTES: 1. All tests performed at TA=125°C may, at the manufacturer's option, be performed at TA=150°C.
 - Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.
 - 3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.38. Electrical performance characteristics for device type 04 (LM137K) (See 3.4 unless otherwise specified)

	1	Condition: (Fig. 12 unless	otherwise	1		
Characteristic	Symbol		tated)	OCHEIWISE	1.1	mits	(
	1		Load Current	Other			Units
Output Voltage	VOUT	VIN=-4.25V	IL=5mA,1500mA		-1.300		
		VIN=-41.25V	IL=5mA,200mA	_	1	1	}
_	ł	VIN=-6.25V	IL=5mA	TA=150°C 1/	1	l	[
Line regula-	VRLINE	-41.25V VIN	IL=5mA	TA=25°C	- 9	9	.mV
tion	} <u>-</u>	4-4.25V		-55°C≰TA	}		1
				≤ 125°C	-23	23	!
Load regula-	VRLOAD	V _{IN} =-6.25V	5mA FIL 1500mA		- 6	6	1
tion	1			-55°C4TA	-12	12	ì
				≤ 125°C			1
		VIN=-41.25V	5mA=IL=150mA	TA=25°C	- 6	6	Ì
	1			-55°C ≄ TA	-12	12	ĺ
				≟ 125°C			ł
Thermal regu-	VRTH.	V _{IN} =-14.6V	I_L =1500mA	TA=25°C	- 5	5	l
lation			_]			1
Adjust pin	IADJ	VIN=-4.25V	I_L =5mA		25	100	μA
current		V _{IN} =-41.25V	IL≖5mA		25	100	
Adjust pin	4 I _{ADJ}	-41.25V≰I _{I.} €	IL=5mA		- 5	5	
current	(LINE)	4.25V		{			,
change versus							
line voltage							
Adjust pin	△ IADJ	$V_{IN} = -6.25V$	5mA 41 41 500mA		- 5	5	
current	(LOAD)			{			
change versus	ĺ ` .			•			
load current	•			}	i '		
Minimum load	IQ	-14.25V TN			0.20	3.00	mA
current		4-4.25 V		. ·	1.00	5.00	
		forced Vour					
	<u> </u>	=-1.4	_	1			
		V _{IN} =-41.25V			1.00	5.00	
	}	forced Vour					
		=-1.4V					
Output short	I _{OS} 1	V _{IN} =-4.25V			1.5	3.5	A
circuit cur-	IOS2	VIN=-40V	,		0.2		A
rent	1			<u>l</u> `			
Output volt-	VOUT	VIN=-4.25V	RL=.8334;CL	After IoS1	-1.300	-1.200	V
age recovery	(RECOV)		F بر20=	$\frac{1}{2}$	Ì		
after output	1	VIN=-40V	R _L =250	After Ios2			Ì
short circuit							· ·
current					ł i		
Voltage start-	VSTART	VIN=-4.25V	R _L =.833a;C _L]	-1.300	-1.200	
up	1		=20µF				
	AVIN	VIN=-6.25V	IL=500mA	Figure 13	50		dB
tion		C _i =1Vrms		TA=25°C	ł i		
		@fo=2400Hz					
Output noise	VNO	V _{IN} =-6.25V	I _L =100mA	Figure 14		120	ųV rms
voltage	Ì		, -	TA=25°C			
	1			BW=10Hz to			
	1			10kHz			
	<u> </u>		III-107				·

Table 3.38. Electrical performance characteristics for device type 04 (LM137K) (Cont'd) (See 3.4 unless otherwise specified)

		Condition: (Fi	g. 12 unless	otherwise			
Characteristic	Symbol	stasta	ted)		Li	mits	
		Input Voltage	Load Current	Other	Min.	Max.	Units
		V _{IN} =-6.25V AV _{IN} =-1.0V		Figure 15 TA=25°C		40	mV/V
Load trans-	∆ VOUT ∆ IL	V _{IN} =-6.25V	IL=100mA	Figure 16 TA=25°C		0.15	mV/mA

- NOTES: 1. All tests performed at $T_A=125\,^{\circ}\text{C}$ may, at the manufacturer's option, be performed at $T_A=150\,^{\circ}\text{C}$. Specifications for $T_A=125\,^{\circ}\text{C}$ shall then apply at $T_A=150\,^{\circ}\text{C}$.
 - 2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.
 - 3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

SECTION IV

MULTIPLE Bi-FET OP AMPS MIL-M-38510/119

TABLE OF CONTENTS

		Page
4.1	Background and Introduction	IV-1
4.2	Description of Device Types	IV-2
4.3	Device Characterization	IV-7
4.4	Tabulation of Test Data	IV-8
4.5	Discussion	IV-8
4.6	Conclusions and Recommendations	IV-11
4.7	Ribliography	IV-11

LIST OF FIGURES AND TABLES

Figure	Title	Page
4-1	TLO61 Series Op Amp Schematic	IV-3
4-2	TL071 Series Op Amp Schematic	IV-4
4-3	uAF771 Series Op Amp Schematic	IV-5
4-4	LF151, 153, 147 Op Amp Schematic	IV-6
4-5	Common Mode Rejection Histogram	IV-24
Table		
4-1	Typical type 02 data at 25°C	IV-12
4-2	Typical type 02 data at -55°C	IV-13
4-3	Typical type 02 data at 125°C	IV-14
4-4	Typical type 05 data at 25°C	IV-15
4-5	Typical type 05 data at -55°C	IV-16
4-6	Typical type 05 data at 125°C	IV-17
4-7	Statistical data of types 01, 02 & 03 at 25°C	IV-18
4-8	Statistical data of types 01, 02 & 03 at -55°C	IV-19
4-9	Statistical data of types 01, 02 & 03 at 125°C	IV-20
4-10	Statistical data of types 04, 05 & 06 at 25°C	IV-21
4-11	Statistical data of types 04, 05 & 06 at -55°C	IV-22
4-12	Statistical data of types 04, 05 & 06 at 125°C	IV-23
4-13	Proposed MTI-M-38510/119 electrical characteristics	TV-25

SECTION IV

MULTIPLE Bi-FET OP AMPS MIL-M-38510/119

4.1 Background and Introduction

The first op amps of this series which were introduced to RADC for characterization and possible slash sheet action were the TL061 and TL071 families from Texas Instruments. Each of these families included single, dual and quad device types. The TL061, TL062 and TL064 devices were offered as a low power category and the TL071, TL072 and TL074 devices were classified as low noise devices. Preliminary characterization studies at GEOS were encouraging and a recommendation for slash sheet action was made. Since these new Bi-FET op amps had lower absolute maximum ratings than the LF155 series devices, it was necessary to generate a new slash sheet. National Semiconductor and Fairchild were also introducing multiple Bi-FET op amp devices which could be included in the new slash sheet. MIL-M-38510/119 contains the following generic industry devices:

Generic Industry Type Mil	itary Device Type
TLO61 (single-low power)	01
TL062 (dual-low power)	02
TL064 (quad-low power)	03
TLO71, uAF771, LF151 (single - general purpose)	04
TL072, uAF772, LF153 (dual - general purpose)	05
TL074, uAF774, LF147 (quad - general purpose)	· 06

The differences between the absolute maximum rating of the /114 and /119 military specifications are shown below:

MIL-M-38510-/114	<u>/119</u>
± 22v	± 18V
	± 15V ± 30V

^{1/} The absolute maximum negative input voltage is equal to the negative power supply voltage.

Whereas device types 01, 02 and 03 are intended for low power applications, device types 04, 05 and 06 are intended to be the future low cost "741 work horses" of the industry.

4.2 Description of Device Types

The op amps specified in /119 have fewer J-FETs per op amp than the LF155 series devices. As a result the chip real estate per function is approximately 2/3 that of an LF155 device. Consequently, the options for lower cost and multiple op amp devices are also more viable than with the LF155 series design.

Figures 4-1, 4-2, 4-3 and 4-4 show the schematic diagrams of these new second generation Bi-FET op amps. All of these devices feature J-FETs for the differential input stage and complementary bipolar transistors for the totem pole output stage. Unlike the LF155 series design a J-FET is not used to replace the output PNP transistor for stability improvement.

Another common difference between these devices and the LF155 series is that the input J-FETs are not loaded by matched J-FET current sources. Instead a bipolar current mirror is used with trim resistors in the emitter legs. Offset voltage can be internally laser trimmed or externally potentiometer trimmed. Because of pinout restrictions some of the duals and all of the quads do not have external offset voltage adjustment capability. Caution should be exercised in swapping /119 single with /114 devices in applications using the offset control pins.

Since the LF155 adjustment is connected to + $V_{\rm CC}$ and the /119 single device is connected to - $V_{\rm CC}$ proper operation after swapping will not work and could lead to device destruction if the trim wiper gets too close to one of the potentiometer ends.

The input for the single ended high gain second stage is taken off the collector of the current mirror transistor.

Another current mirror connected to a zener regulated current source provides separate constant current biasing for the first and second amplifier stages of the TLO71 series devices.

The current source stage biasing for the other devices are all different in design. Modifications of current mirrors and lateral PNP transistors are used extensively as can be seen in the circuit schematics. The degree of circuitry used for stage biasing enables the op amps to be used over a wide range of power supply voltages while maintaining excellent power supply rejection to noise and other disturbances. Further details are covered in the manuals, books and papers referenced in the bibliography of this report.

All of the generic industry device types within the /119 specification have design differences which will tend to favor one parameter over another. As a consequence of this fact the margin of performance between the different vendor devices and the specification limits will vary accordingly.

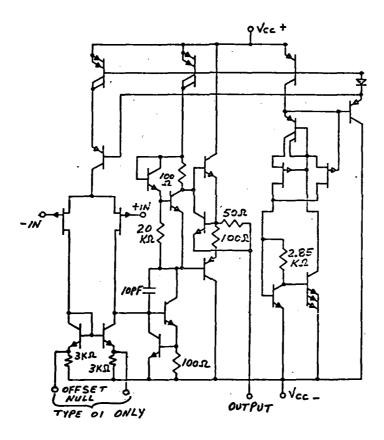


Figure 4-1. TLO61 Series Op Amp Schematic.

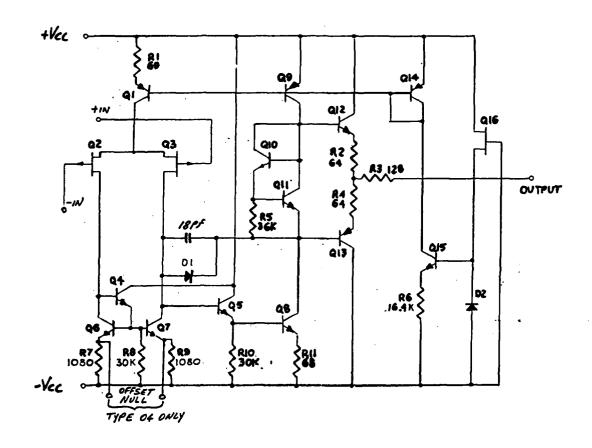


Figure 4-2. T1071 Series Op Amp Schematic.

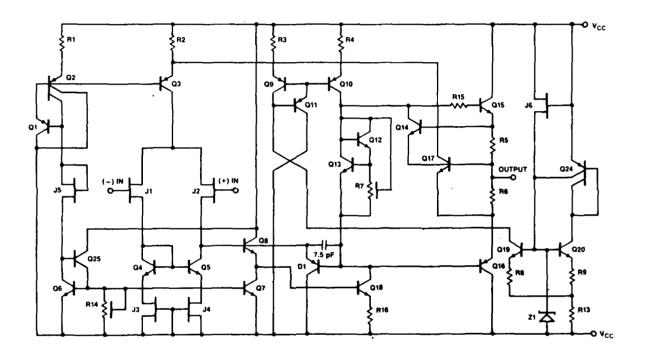


Figure 4-3. uAF771 Series Op Amp Schematic.

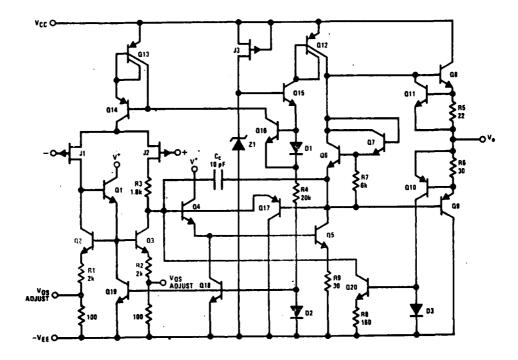


Figure 4-4. LF151, 153, 147 Op Amp Schematic.

4.3 Device Characterization

The characterization procedure for the multiple Bi-FET op amps was very similar to the procedure described in Section 2.3. A notable difference was that the test adapter had to be configured to accept dual and quad devices in addition to single devices. This was accomplished by building several DIP to TO5 pin-out converters with manual selection switches. Although this method was satisfactory in getting the data, a more elaborate relay controlled socket would have been more efficient for testing large quantities of devices, especially if this effort were required on a continuing basis.

Software changes were made to the program to reduce the power supply and command voltages to the specified values for these devices. Transient response, settling time and slew rate data were measured manually with a new test fixture having dedicated DTP sockets for single, dual and quad devices.

As with the LF155 series devices, a Tektronix 577 curve tracer was used to observe parameter to parameter characteristics of sample devices. Further details on op amp characterization test procedures are contained in Section 2.3.

4.4 Tabulation of Test Data

A representative tabulation of S-3260 characterization data is shown in Tables 4-1 through 4-6. Each of these data sheets show how the data values of 10 devices compares to the JC-41 Committee limits at a given test temperature. Most parameters were tested with ± 16 volt power supplies over a \pm 12 volt common mode range. Even though device types 01, 02, and 03 are not rated to drive a 2000 ohm load, data was taken with this condition for information only.

Statistical summaries of all the data are shown in Table 4-7 through 4-12.

Histograms were generated on an op amp basis for both device type families for all parameter-temperature combinations. One such histogram at 25°C of common mode rejection for device types 04, 05 and 06 is shown in Figure 4-5.

A complete tabulation of the data is being issued in handbook form to the JC-41 Committee representatives.

4.5 Discussion

The characterization data was carefully reviewed to determine how well it complies to the proposed JC-41 limits and the June 1979 Rev. 1 issue of MIL-M-38510/119. Where there is good agreement between the data and the limits, no further discussion will be given here. The proposed JC-41 parameter limits will then be carried over into Table 4-13. Where there is a discrepancy between the data and the JC-41 limits a discussion will be included with GEOS proposed limits. Because of the limited sample size (51 low power op amps and 81 low cost op amps), the GEOS data may not accurately reflect the data of all manufacturer lot samples.

Vendor feedback will be required before firm limits can be recommended for the proposed multiple op amp slash sheet MIL-M-38510/119. Table 4-13 is the best estimate of this time of the /119 Table I limits.

4.5.1 Input Offset Voltage (Vio)

With the exception of vendor B Type 04 devices at 125°C, the offset voltage data agrees with the proposed limits of \pm 5 mV and \pm 7 mV at 25°C and over the military temperature range, respectively.

4.5.2 Input Offset Current (I10)

Early in the characterization program there were many device failures to the \pm 50 pA JC-41 limits. Because of this the histogram and statistical analysis limits were loosened to \pm 100 pA. A comparison of the 25°C, zero common mode offset current data against the data limits is as follows:

4.5.2 Input Offset Current (Iio) (cont.)

Device Type	Yield @ $I_{io} = \pm 100 \text{ pA (max)}$	Yield @ I _{io} ± 50 pA (max)
01,02,03	(51-8)/51 = 84%	(51-15)/51 = 70%
04,09,06	(81-18)/81 = 78%	(81-27)/81 = 67%

For reasonable yields the ± 100 pA limits should be used.

4.5.3 Input Rias Current (± IiB)

At the negative common mode condition at 25°C, both device families had yields of less than 70% against the -200 pA limit. The yields improve to better than 80% with a relaxed low limit of -400 pA. The high temperature high limits were too loose and it is suggested that they be changed from 100 nA to 70 nA at the positive common mode voltage and from 70 nA to 50 nA for the other common mode voltage conditions.

4.5.4 Short Circuit Current (Ios(+), Ios(-)

Based on these devices alone limits of 30 mA would be recommended; however, other vendor type devices, not yet characterized, require the 40 mA limit for the low power category. The general purpose device limits of \pm 80 mA are reasonable.

4.5.5 Supply Current (Icc)

Although the supply current is specified on an op amp basis, observations of the data show that duals and quads use less current per op amp than does a single device. An average "discount" for the multiple op amps based on histogram mean values is 20% for the duals and 30% for the quads. No change is recommended for /119.

4.5.6 Output Voltage Swing (+ Vop, - Vop)

Based on the data, the voltage swing limits are specified very conservatively. For device types 01, 02 and 03 with a 10K ohm load, $-V_{op}$ is the weakest drive. 50 out of 51 devices had less than 1.2 V of negative saturation. $(-V_{sat} = |-V_{cc} - (-V_{op})|)$.

The single 01 maverick with 1.7 V of negative saturation also failed the V_{io} , -PSRR and the gain tests. For the 04, 05, and 06 device data the maximum saturation drops were 2.1 V at 10 K Ω and 3.5 V with 2K Ω loading.

4.5.6 Output Voltage Swing (+VOP, - VOP) (cont.)

It is recommended that the swing limits be increased to 12.5 V at 10K and 11 V at 2K. The characterization data was measured with $\pm \text{ V}_{\text{CC}} = \pm 16 \text{ V}$, whereas the proposed slash sheet is specified with $\pm \text{ V}_{\text{CC}} = \pm 15 \text{ V}$. Because of this difference the data was examined on an "output to rail" basis.

4.5.7 Open Loop Voltage Gain (Avs (+), Avs (-))

One of the tradeoffs for device types 01, 02 and 03 is that the low power option results in lower open loop gain. One change that can be recommended is that AVS at \pm V_{CC} = \pm 5 V be increased from 2 to 3 V/mV (min.). The lowest corresponding data value was approximately 4.8 V/mV from a -55°C histogram.

As a general observation, device types 04, 05 and 06 have lower gains than the 155 series devices by a factor of from 1/4 to 1/3.

4.5.8 Slew Rate (SR(+), SR(-))

With the exception of several failures from vendor code B devices, all of the devices had slew rates greater than the specified minimum levels. No specification change is recommended, unless vendor code B determines that a relaxation in limits is necessary.

4.5.9 Transient Response (TR(tr), TR(os))

The previous parameters were measured automatically, but transient response was measured manually with a signal generator and an oscilloscope. Histograms were generated on the S-3260 from the manual data.

For the low power devices the data indicates that the rise time and overshoot should be changed from 600 nanoseconds and 40% to 400 nanoseconds and 20% respectively. These limits would still leave a 2:1 margin from the observed worst cases. Device types 04, 05 and 06 have data in good agreement with the limits.

4.5.10 Settling Time $(t_s(+), t_s(-))$

The data indicates that the settling time limit for device types 01, 02 and 03 need to be increased from 1500 ns to 6000 ns. The initial limits of 1500 ns was a tentative estimate without a JC-41 recommendation.

In view of the fact that device types 04, 05 and 06 have four to five times as fast a slew rate as the low power devices, it is not surprising that the data yields a similar conclusion with settling time.

4.6 Conclusions and Recommendations

A characterization study was conducted on a mix of single, dual and quad Bi-FET op amps. The data base consists of 51 low power op amps and 81 general purpose op amps. Minor changes in the JC-41 specifications were made to reflect GEOS's data observations, yield considerations and user priorities. These multiple Bi-FET op amps should find many useful applications in military systems.

4.7 Bibliography

- 4.7.1 R. Russell and T. Frederiksen, "How the Bi-FET process benefits linear circuits," Electronics, June 8, 1978.
- 4.7.2 Bi-FET op amp family from Texas Instruments, Bulletin CB-24B
- 4.7.3 Linear Applications Handbook, National Semiconductor (1978)
- 4.7.4 Linear Databook, National Semiconductor (1978)
- 4.7.5 Signetics Analog Data Manual (1977)

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SE NIMI-	ŧ	OUT S	,	14.3.3 2.4.3.3		107.	168.	- 6 .15 5.65	30.E	2.4.4. 0.4.4.	2.7.2.2. 2.7.2.2.2 2.7.2.2.2 5		NO LIMIT
TANE:		2222 	•	• •	•	88 8.0 6.7	87.7	-8.76 5.85	335.MX	1.4.9 1.4.9 1.4.9		**	UTN PEAN
, DEVICE	E 7-07	****	****			22	2	7.0			******	***	INITS COL
HANDFACTURER COBE: A 5	PARACETER	U10(-CR) AT 890, 40 U10(-CR) AT 40, 489 U10(-CR) AT 180, 180 U10(-CR) AT 90, -0.0 B-U10/P-T FROM 85 OC	110(-CH) AT 289,-40 110(+CH) AT 40,-280 110(+CH) AT 180,-180 110(+CH) AT 80,-280	+IIB(-CR) AT 280,-40 +IIB(+CR) AT 40,-280 +IIB(+CR) AT 160,-160 +IIB(+CR) AT 80,-240	-IIB(-CM) AT 280,-40 -IIB(+CM) AT 40,-280 -IIB(+CM) AT 150,-160 -IIB(+CM) AT 80,-240	+PSRR AT 80,-160 -PSRR AT 160,-80	CHR AT 16U,-16U	105(+) AT 150,-150 105(-) AT 150,-150	ICC AT 150,-150	+00 AT R1-19K +00 AT R1-19K +00 AT R1-2K -00 AT R1-2K	AV5(+) AT RL-10K AV5(-) AT RL-10K AV5(-) AT RL-0K AV5 AT BV,-BV,RL-10K AV5 AT BV,-BV,RL-10K AV5 AT BV,-BV,RL-10K	9R(+) AT 160,-160 9R(-) AT 160,-160	NOTES:1.2ERO (8) IN LIMITS COLU

Table 4-1. Typical type 02 data at 25°C.

	F15	£ £ ££\$	3333	3333	1111	44	7	٤٤	£	>>>>	>>>>>> 555555	22 22
	M1-11	*****	****	****	****	**	:	**	E.	10.80	*****	** **
		######################################	****	****	****	87.4 87.4	8.78	6.15	285,H	15.0 -14.8 13.3 8.35 8	2.00 2.00 2.00 2.00 2.00 2.00 2.00 2.00	22
	1	22723	****	****	::::	83.5 23.5	105.	-11.1 6.45	285.4	15.0	2.4.5.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1	 22
10.86:32	ŧ	****** ******	****	****	****	804.S	87.0	-11.6 6.65	295.R	9.3.5.9 • 3.5.6 • 3.5.0		<u></u>
	2	2000 2000 2000 2000 2000 2000 2000 200	****	****	****	166. 86.1	88.3	-11.4	305.H #	-15 -14 -9.6 -9.6		87
C , 27 SE	Ī	14148 16818 EEEEE	****	****	****	8 3.8	110.	-11.6	285.R			1:87 1:87 1:86 1:00
TEMPERATURE: -66 DEG C , 27 SEP 79	Ĭ		****	****	****	95.1 86.5	97.9	-11.5	38.3 x	2.4.0.0 0.00.00 0.00.00	204804 278290 278290	25 S
PERATURE:	į	E 98	****	****	2223	9:.2		6. % 5. %	350.N B	# # # # # # # # # # # # # # # # # # #	2945 285 285 285 285 285	1.07 1.16 1.15
2 , TEM	2	¥-885	****	****	****	94.5 103.	87.8	-0.6 -0.5 -0.5 -0.5	296.A	-11.5. -2.11.0. -2.11.0.		28 55 10 54 11 55 12 55 13 55 14 55 15 15 15 15 15 15 15 15 15 15 15 15 1
- DUAL-	Ī	1278- 6168- 6166-	****	****	****	101.	.	5.35	386.H #		######################################	1.68 2.17 70 LIMIT.IT
	ž		****	****	****	92.5	87.4	-11.9	305.N x		**************************************	2k A
MUICE	LO-LIN	*****	****	****	****	**	:	***	•	2020	******	### SET
MANUFACTURER CODE: TT,	PARAMETER	V10(-CH) AT BBU, -40 V10(-CH) AT 4U, -88U V10(-CH) AT 4U, -18U V10(-CH) AT 5U, -5U B-U10/D-T FROM BE OC	110(-CH) AT 280,-40 110(+CH) AT 40,-280 110(+CH) AT 180,-160 110(+CH) AT 80,-240	+IIB(-CR) AT 880,-40 +IIB(+CR) AT 40,-280 +IIB(+CR) AT 160,-160 +IIB(+CR) AT 80,-240	-IIB(-CR) AT 880,-40 -IIB(+CR) AT 40,-280 -IIB(+CR) AT 160,-160 -IIB(+CR) AT 80,-240	+PSRR AT 80,-160 -PSRR AT 160,-80	CMR AT 16U,-16U	10S(+) AT 15U,-15U 10S(-) AT 15U,-15U	ICC AT 150,-150		835(+) AT R[-196 835(+) AT R[-196 835(+) AT R[-186 835(+) AT R[-186 835 AT B[-196 835 AT B[-196, R[-196	SR(-) AT 18U,-18U SR(-) AT 18U,-18U HOTES:1.2ERO (0) IN LINITS OF

Table 4-2. Typical type 02 data at -55°C.

MANUFACTURER CODE:		J.	2 PM-	1	TEMPERATURE	*186 960	# 18 TO	2 22	18:33:17				
PARAMETER	10-LIN	ä		2	ž	£	Ĭ	2	Ī	2	•	HI-LIM	2115
UID(-CH) AT 880, -40 UID(-CH) AT 180, -180 UID(-CH) AT 180, -180 UID(-CH) AT 80, -80 B-UID/P-T FROM 86 OC	*****	27.22 27.22		71578	40042 40042		48494 4864 6666 6666	6 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	******			\$\$\$\$\$°	25553 6
IIO(-CR) AT 880, -40 IIO(+CR) AT 40, -880 IIO(+CR) AT 160, -160 IIO(+CR) AT 80, -240	****	#144 ##£#		1141 2411	****					11.14 11.14 11.14 11.14 11.14 11.14	-1.67 -1.67 -1.38 -1.31 -1.31	****	1111
+IIB(-CR) AT 880,-40 +IIB(-CR) AT 40,-880 +IIB(-CR) AT 160,-160 +IIB(-CR) AT 80,-240	****	13.55 13.55	****** *****	14.5K 13.58K 13.58K	27.38 27.38 37.38	50.00 50.00	200 00 00 00 00 00 00 00 00 00 00 00 00	6.3.6.4 6.3.8.4 1.5.4 1.5.4	7.54 7.54 6.61 6.61 6.61 6.61	4000 4000 4000 4000 4000 4000 4000 400	#### ####	5855 8488	1111
-IIB(-CR) AT 280,-40 -IIB(-CR) AT 40,-280 -IIB(-CR) AT 160,-160 -IIB(-CR) AT 80,-240	****	-2.00 -2.00 -2.00 -2.00 -2.00 -2.00 -2.00 -2.00 -2.00 -2.00 -3.00	-36.34 -2.38 -2.38 -2.38 -2.38 -3.38	-33.8K # 35.6K -1.41K 84.7K	-18.5K # 31.1K 4.33K 23.6K	-359. 9.21K 9.22K 6.82K	1.17 1.02 1.03 1.03 1.03 1.03 1.03 1.03 1.03 1.03		2.31K 10.7K 6.15K 9.52K	9.94 9.94 9.864 9.894	1.77K 10.1K 5.36K 8.76K	\$3.55 \$4.55	4444
+PSRR AT 80,-160 -PSRR AT 160,-80	**	83.7	91.2 103.	4.0	95.1 163.	 	 	7.C.	89.0 115.	92.3 118.	89.3 96.1	33	44
CNR AT 160,-160	.	8.3	36 .1	8 .	91.0	102.	109.	87.8	96.6	88.1	8.5		#
105(+) AT 15U,-15U 105(-) AT 15U,-15U TCC AT 15U,-15U	** **	-5.25 4.45	\$0.4 \$0.4 \$0.4	-5.05 4.15	2 2	5.36	-5.50 4.75	-5.70 4.80	-5.55 4.50	-5.50 4.45	-5.50 4.05 8.05 8.05		\$
+UOP AT RL-19K +UOP AT RL-19K +UOP AT RL-2K -UOP AT RL-2K	.8.8	24.0 24.0 24.0 24.0	77.00	2.0.0. 2.0.0. 2.0.0. 3.0.0.	15.3 -14.7 9.65 #	11.00	15.3 -14.8 -7.85 #	11-15 10-15	114.00 14.00 14.00	-7.35 a	2.00 2.00 2.00 2.00 3.00 4.00 4.00	3.8.	2222
AVS(+) AT RL-19K AVS(-) AT RL-19K AVS(+) AT RL-3K AVS(-) AT RL-3K AVS AT SV, -SV, RL-19K AVS AT SV, -SV, RL-19K	******	### FE	** ** ** ****** *******	**************************************		24.40.00 0.00.00.00 0.00.00.00 0.00.00.00	4 20 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		0.44.00. 0.6.4.00. 0.6.4.00. 0.4.00. 0.4.4.4.4.4.4.4.4.4.4.4.4		20.00 20.00		22222 222222 222222
88(+) AT 180,-180 88(-) AT 180,-180	\$8	46 94	 9.9	ei Er	22	## ##	#8 #8	22	#3 #4	86. 88.	44 44	22	55
NOTES:1.ZERO (0) IN LIMITS COL	ITS COLL	TH RANG	NO LIMIT.	THE CASE DE	INTERPRE	TED AS A	DASH (-).						

Table 4-3. Typical type 02 data at 125°C.

	15	5555 3	2223	2223	2222	44	7	٤٤	£	>>>>	22222 232223	55
	HI-LIM	*****	<u> </u>	**************************************	% 	32		**	8	 8.8.	*****	** **
	7-925	85588	6.00 6.00 6.00 6.00 6.00	8.66 357. 128. 200.	-21.7 229. 65.8 140.	28 20 20 20 20 20 20 20 20 20 20 20 20 20	94.9	-21.6 19.8	3.62	2111 6444 0400		19.1
	1-989	 	85.85 9.00.00	-115. 333. 83.1 801.	-195. 46.8 228.	109.	112.	-21.6 18.8	3.60 1	7.4.4.4 0.4.00	3 44±3±	7 4
14:47:83	1-18	#45#8 #45#8	2000 2000 2000 2000 2000 2000 2000 200	6.50 8.00 8.00 8.00	-4.31 294. 58.4 118.	118. 89.3	83.9	-21.4	3.68 *	N444 N400	13423	
BE 79	/- 189	55.223 5.223 5.223	58.8 -83.4 -3.37 -13.6	-117. 334. 38.2 162.	-169. 357. 35.5 175.	98.5	86.8	-21.5	3.71 \$	N.4.4. 0.4.00		
0 C , 26 SEP	2- c e s	2228 2228	200 200 200 200 200 200 200 200 200 200	# 436. 824. *	-17.5 218. 57.4 129.		97.6	-20.6 18.5	3.61 *	0.444 -4.400		17:9 17:9 10:4
E: +26 DE0	/- 025			-73.9 396. 44.8 154.	-98. 367. 263.	86.5 2.1.	102.	-20.8	3.65 *	7444 0444 0400	# #	12.51 13.51 14.0 AS A
TEMPERATURE:	7-889	44449 22528	11.1.4 10.0.4 10	-45.8 -78.0 -61.7	-39.9 266. 59.6 146.	100. 88.2	85.1	-20.7 18.0	3.78 \$	0141 0444	\$\$\$£\$\$	17.8 18.8
-)- 25	initio Viinis	4. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.	-163. 703. 812.	-199. 463. 69.5 256.	101.	93.1	-19.9	3.76 #	14.4.1		
163 DUAL	# - 1 29	27578	8446 6466 6666 6666 6666	223. 38.1 126.	-57.7 269. 62.0	92.5 92.7	102.	-22.2 19.8	3.83 #	2444 2444 2464		SECTION CINE
1	E 581:-1	28:48	- C	-19 869. 1869.	-31.0 272. 68.8 162.	85.0 84.7	93.4	-22. • 19.8	3.84 x	0444 4409	######################################	16.7 19.8
DEVICE	17-07	*****	#### #####			88.0	89.0	-8	:	 		28. ST
MANUFACTURER CODE: TT,	PARAMETER	U10(-CH) AT 88V,-4V U10(-CH) AT 4V,-88V U10(-CH) AT 18V,-18V U10(-CH) AT 8V,-6V B-U10/P-T FROM 25 OC	IIO(-CR) AT 880,-40 IIO(+CR) AT 40,-280 IIO(6CR) AT 160,-160 IIO(+CR) AT 80,-240	+IIB(-CR) AT 280,-40 +IIB(+CR) AT 40,-280 +IIB(+CR) AT 160,-160 +IIB(+CR) AT 80,-240	-IIB(-CR) AT 280,-40 -IIB(-CR) AT 40,-280 -IIB(-CR) AT 160,-160 -IIB(-CR) AT 80,-240	+PSRR AT 80,-160 -PSRR AT 160,-80	CMR AT 16U,-16U	105(+) AT 15U,-15U 105(-) AT 15U,-15U	ICC AT 15U,-15U	+UOP AT RL-16K -UOP AT RL-16K +UOP AT RL-2K -UOP AT RL-2K	AUS(-) AT RI-19K AUS(-) AT RI-19K AUS(-) AT RI-18K AUS(-) AT RI-8K AUS AT BU, -UV, RI-16K AUS AT BU, -UV, RI-16K	90(+) AT 18U,-18U 7.00 90(-) AT 18U,-16U 7.00 NOTES:1.ZERO (0) IN LINITS CO

Table 4-4. Typical type 05 data at 25°C.

	5	5555 3	2333	2222	2233	==	=	££	£	>>>>	333333 \$55555	55	
	MI-LIM	*****	****	2222	****	**	:	** **	3.5	**************************************	*****	\$\$	
	2-899		****	3222	****	97.6	97.2	-26.8 27.0	x 3.67 x			18.	
		*****	****	****	****	93.7	104.	-27.7	3.68		******	17.7	
14146117	2-78		****	****	****	163.	85.9	-27.1 26.4	1 3.79 1		******	17.9	
2 2	3	1400. 1400. 1600. 1600.	****	****	****	95.1 1 0 5.	88.1	-27.9 26.5	13.81	844E	328333 375335	17.6	
	2.03		****	****	****	97.6 96.5	102.	-85.7 55.6	3.65	844. • 5.44. • 5.44.		7.0	C HONG
TEMPERATURE: -56 DEG	2	2000 1000 1000 1000 1000 1000 1000 1000	****	****	****	96.5 8.5	97.6	-86.9 -86.9	3.76		******	15.6	INTERPRETED AS A
TIPERATUR	7- 25	87837 6-667	****	****	****	2.5 2.8	₩9.4	6.00 0.00	3.85	0.4.4.C.	\$\$7728 8	17.6	E INTERPR
-	3	\$8287 77777	3333	****	****	95.8 107.	93.4	- 9 - 9 - 9 - 9	3.88	0444 0440		17.0	NO LIMIT. IT CAN B
163 BUAL	7-189	4444 4444 4444	****	****	****	93.2	8.8	-21.4	# 3.93	2121 8446 6486	22.08C	20	_
-	- ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ;		3323	****	****	gg Ga		. 65. 6.7.	3.86	0444 0440		71. 10.	-
PE V10 E	11-67	*****	****	****	****	22	.00	***	8	######################################	######	**	
MANUFACTURER CODE: TT,	PROPERTY	VIO(-CH) AT 88V4V. VIO(-CH) AT 4V88V. VIO(-CH) AT 18V18V VIO(-CH) AT 8V8V. P-VIO/-P-T FROM 85 OC	110(-CH) AT 880,-40 110(-CH) AT 40,-880 110(-CH) AT 160,-180 110(-CH) AT 80,-840	+IIB(-CH) AT 280,-40 +IIB(+CH) AT 40,-280 +IIB(+CH) AT 160,-160 +IIB(+CH) AT 80,-240	-IIB(-CR) AT 280,-40 -IIB(-CR) AT 40,-280 -IIB(-CR) AT 160,-160 -IIB(-CR) AT 80,-240	+PSGR AT 80,-160	CHR AT 160,-160	105(+) AT 15U,-15U 105(-) AT 15U,-15U	ICC AT 15U,-15U	+107 AT R1,-18K +107 AT R1-18K +107 AT R1-18K	AUS(+) AT RL-16K AUS(-) AT RL-16K AUS(-) AT RL-20K AUS(-) AT RL-20K AUS AT SU, -EU, RL-16K AUS AT SU, -EU, RL-36K	8R(+) AT 16U;-16U 8R(-) AT 16U,-16U	NOTES11.ZERO (8) IN LINITS CO

Table 4-5. Typical type 05 data at -55°C.

	\$11P	5555 3	3333	2222	2222	Çŧ	7	£ £	£	>>>>	333333 55555	55
	HI-LIM	*****	****	5255 87.22	\$3.55 \$3.55	**	•	**	8	*****	*****	**
	2- 929	*****	 \$34%	2.9% 21.5% 26.3% 20.3%	23.5 2.3 3.8 3.8 3.8 5.8	106. 105.	93.9	-14.1	2.73	244 244 244	WASTERS 5.5.5.5.5.5.5.5.5.5.5.5.5.5.5.5.5.5.5.	
_	558-t-	######################################		3%≅8 8.8.8.9 9.8.9.9	25.5% 10.5%	118.	124.	-14.0 9.55	1 2.85	01-11 0444 0.00		
14:48:18	2-119		40000 40000 40000 40000	3.94 7.83 9.83 9.83 9.83 9.83	4.10X 11.88X 10.81X 10.81X	93.5	82.9	14.6	¥ 3.03	2444 2444	*****	70
8EP 79	7 72	17867 77977	1.000 1.000 1.100 1.000		10 10 16 14 16 17 17	103. 95.1	86.7	-13.9 9.75	3.28	21.1. R444 W.COU		•
MEG C 1 B6	5- CB9	4432.	#### ####	***** *****	8.38K 17.5K 13.1K 16.1K	184. 102.	86. 7	-13.5 9.85	# 8.8	21.11 04.44 ucom	7.22.22 7.22.22	16.4 16.4
H: 1185 1	E2 3 - C		-1.56K -457. -1.15K -599.	12.34 2.34 2.44 2.44	4.64K 12.7K 8.78K 11.6K		109.	14.3	8	0141 0444 W.COM	######	16.1 15.8 17.8 17.8 INTERPRETED AS A
TEMPERATURE: +125 DEG	7- 868	##### #####	440. 450. 450. 450.	4.0 4.0 4.0 5.0 5.0 5.0 5.0 5.0 5.0 5.0 5.0 5.0 5	4.56K 14.5K 9.65K 13.1K	95.4 96.5		14.1	1 2.57	0141 0444 0400		16.1 17.8 1 Interes
•	3	 6:4:8		2.55 2.95 2.95 2.95 2.95 2.95 2.95 2.95	4.8 4.7 13.7 13.4 4.4	184. 98.5	94 .3	-13.9	3.31	2121 2444 2400		17.6 17.6
183 DUAL	2-188		*****	 *****	5.25K 17.8K 11.8K 16.9K	100	124.	-15.4	1 2.74	N.444		
1 Jent) - I 28	*****	######################################		25.25 25.45 25.45	103. 112.	80.5	-16.0	3.15	0444 U.OU	\$25.128 \$1.17.1.	16.1 18.8 JPT PEANS
DEVICE	10-114	*****	****	****	****	**		÷:	:	.8.8	REBESS.	
MANUFACTURER CODE: 17,	PARAMETER	U10(-C3) PT 880,-140 C10(-C3) PT 40,-180 C10(-C3) PT 180,-180 U10(-C3) PT 80,-10 B-U10/B-T FROM 25 OC	IIO(-CH) AT 880,-40 IIO(-CH) AT 40,-880 IIO(-CH) AT 160,-160 IIO(-CH) AT 80,-840	+118(-CR) AT 280,-40 +118(-CR) AT 40,-280 +118(-CR) AT 160,-160 +118(-CR) AT 80,-240	-IIB(-CB) AT 280,-40 -IIB(+CB) AT 40,-280 -IIB(+CB) AT 160,-160 -IIB(+CB) AT 80,-240	+PSRR AT 80,-160-PSRR AT 160,-80	CMR AT 16U, -16U	105(+) AT 15U,-15U	ICC AT 150,-150	+UOP AT RL-18K -UOP AT RL-18K +UOP AT RL-8K -UOP AT RL-8K	205(+) AT RI-19K 205(-) AT RI-19K 205(-) AT RI-9K 205(-) AT RI-9K 205 AT EV, -EV, RI-19K 205 AT EV, -EV, RI-19K	98(+) AT 18U,-18U 5.00 88(-) AT 18U,-18U 5.00 NOTES11.2ERO (0) IN LIMITS COL

Table 4-6. Typical type 05 data at 125°C.

STATISTICAL DATA FOR ADEVIC	*DEVICE	TYPES	411/119-	01, 02,	03 a	25 DEGREES C	REES C		64 OCT	79	3:48:44				
PARAMETER	LOW	HIGH VALUE	MEAN	SIGHA	SAMPLE	X 1N 2	X IN 3	X FAIL	LOW 1	L0*	LO-FM	X FAIL	HIGH	HIGH	UNITS
	-	1:	.1.	1:1	1:1			2./	;		: :	>.		2	
	***						i	,		:				1	
7	-6.76	6.9	-822.M	2.80	51	94.1		3.92	-5.00	-10.0	1.49	3,92	5.00	10.0	>
A T	-6.50	6.77	-610.W	2.67	2	94.1		1.96	-5.00	-10.0	1.64	1.96	2.00	10.0	>
¥	-6.67	6.70	-717.W	2.12	51	94.1		1.96	-5.00	-10.0	1.57	1.96	5.00	10.0	>
Y	-6.15	7.64	-551.M	5.69	5	94.1		3,92	-5.00	-10.0	1.65	3.92	5.00	10.0	>
AT	-241.	205	-3.20	94.2	46	84.3		6	-100	-300.	1.03		100	300	PA
A	-323.	250.	62.0	95.5	6	92.2		1.96	-300	-690	3.79	2	300.	.009	PA
¥	-230-	155.	-1.03	72.6	20	88.2			-100.	-300	1.36	(E)	100	300	ρA
=	-189.	175.	27.9	5.09	6	88.2		9	-100.	-300.	2,12		100	300	ρĄ
7	-465	164.	-152.	140.	46	84.3		3.5	-500-	-200	343.4	000	200	400	P.A
¥		2.06K	541.	359.	5	94.1		00.0	-200	-200	2.07		1.20X	2.50K	ρĀ
Y T		373.	3,43	86.6	21	45.2		1.96	-200-	-200	2.35	3.65	200.	400	ρA
¥	-213.	324.	169.	84.5	47	2.0%		1.06	-500	-200.	4.37		500.	400	A 9
=	-421.	-37,3	-163.	84.5	89	5.06		6	-200-	-200	M. PO D	00.0	200.	400	ρĄ
¥		1.92K	440	275.	2	96.1		0.0	-200-	-200	2.36	1.96	1.20K	2.50K	Αq
¥		170.	-3.00	39.5	2	96.1		0.00	-500-	-200	4.98	0.00	200	400	δĀ
-IIB(+CM) AT 8V,-24V	70.3	312.	148.	52.3	7	86.3		0.0	-500-	-200	99.9	3.95	500.	.00a	P.
	79.4	18.	62.6	7.83	20	2.06		1.96	90.0	0.09	2.03	0.0	2.00K	140.	F.O
-PSRR AT 16VRV	75.4	124.	91.0	60.6	20	92.2		3.45	80.0	0.09	1.16	0.00	2.00K	140.	96
791-'A91 1V BAD	84.3	128.	95.R	9.56	5	96.1	_	0.0	B0.0	9.09	1.71	0.0	2.00X	140.	: ::
108(+) AT 15V, -15V	-11.8	-R.10	-10.0	1.19	51	100		0.0	-40.0	-100-	25.5	0.0	1.00×	0.00	4
<u> </u>	4.55	9.45	6.93	1.21	2	98.0		0.0	-1-00K	00.0	833.	0.0	40.0	100	4
-	15.1	15.2	15.2	27,14	2 :	98.0	100	0.0	12.0	9.00	117.	00.0	200	16.0	>
	0.0	-14.5	. 14.	2 4 5 6	<u>.</u>	98.0	_	000	500	-16.0	2.20K	0.0	-12.0	-8.00	>
-VOD AT DIESK	9 0	e .	10.6	20.00	7			00.0	10.0	8 00	£.	e(200	9.0	> :
			0,00	000	2	7 00					• • • •		0 0 0	00.0	, > ;
7 7		7 9 7	100	000	7 2		_		0		C 11	200	4 2	00.	^ .
7	7.13	8	7.42	1.22	: :	9.1							¥ ×		> >
7	569.4	26.	3.75	184.4	5	98.0	_	100	00.5	0.00	-22.7		¥ .		
AVS AT 5V,-5V, RL=10h	2.5A	9.30	7.95	1.03	21	98.0	_	00.0	2.00	00.0	5.79	00.0	10.0K	100	\ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
2	M. D96	3.08	2.30	396.M	51	98.0	_	4.5	5.00	0.00	764.M	00.0	10.0K	100	7
¥	762.H	3.38	2.70	492°4	21	98.0	_	9	2.00	0.00	- 1.42	0.00	25.0	40.0	V/US
SR(-) AT 16V,-16V	763.M	6.80	5,30	1.28	51	98.0		1.96	2.00	0.00	5.5 8	0.00	25.0	40.0	\$07A

NOTES: 1./ EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ
2./ % FAIL VALUES >OR= 5% ARE CIRCLED
3./ % FIGURE OF MENTI DEFINITIONS: LO-FM=(MEAN-LOM LIMIT)/SIGMA
4./ THE % FAIL FOR ICC IS NOT VALID SINCE THE DUAL AND OUAD DEVICES
ARE COMPARED TO THE SINGLE LIMIT
5./ THERE IS NO MAXIMUM FAIL LIMIT FOR GAIN AND SLEM RATE

Table 4-7. Statistical summary of types 01, 02 & 03 at 25°C.

STATISTICAL DATA FOS +DEVI	*DEVICE		TYPES MIL/119-01, 02, 03 a -55 DEGREES C	01, 02,	. e £0	-55 DEG	REES C		04 OCT	44	13:55:11				
PARAMETER	LO:4 VAL 115	HIGH	MEAN	SIGMA	SAMPLE	K IN 2	SAMPLE X IN 2 X IN 3 SIZE SIGMA SIGMA	X FAIL LOA	141	L0%	10-FM	X FAIL	H16H	H 1 5 H	UNITS
	1:1		1:	::		·			;	<u>.</u>	:	>.			
				!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!		1 1 1		•		:	!!!	•		:	•
VIO(-CM) AT 24V,-3V	-7.9		-1.40	2.47	0	88.2	96.1		-7.00	-10.0	2.26	1.96	7.00	10.0	>
VID(+C4) AT AV287	-9.3		-1.30	2.59	20	92.2	96.1		-7.00	-10.0	2.20	1.96		6.0	>
VID(054) AT 16V,-167	-9.7		-1.46	2.68	20	92.2	96.1		-7.00	-10.0	2.07			10.0	>
VIO(054) AT 5V,-5V	9.0		-1.29	2.61	50	92.2	98.0		-7.00	-10.0	2.19			19.9	>
+PS44 AT 8V,-16V	84.1	115.	96.2	5,55	20	92.2	96.1	00.0	80.0	60.0	2.91	0.00	2.00X	1.3	ВA
-PSRR AT 16V, -AV	71.		91.1	7.98	21	96.1	98.0		80.0	60.09	1.39			169	R.C
C4R AT 16V16V	82.6		97.3	10.7	5	94.1	100		80.0	60.09	1.62			127.	
108(+) A7 15V,-15V	-14.7		-11.9	1.68	51	96.1	100.		-40.0	-100	16.7			0.33	4
108(-) AT 15V,-15V	2.80		7.00	1.39	51	96.1	98.0		-1.00K	00.0	724.			00.0	4 ×
+VOP AT RL=10K	15.0		15.0	7.004	51	98.0	98.0		12.0	8.00				1.6.0	>
-VOP AT RL=10K	-14.9		-14.8	28.94	50	94.1	98.0		-500-	-16.0				66.00	>
+VOP AT RL=2K	10.2		13.5	1.09	51	94.1	100.		10.0	8.00		000		15.0	>
-VOP AT RL=2K	=		-9.89	861.4	43	94.1	98.0		-500-	-16.0	_			-8.00	>
AVS(+) AT RL=10K	1.6		10.5	1.94	51	96.1	98.0		4.00	0.00				100	?:/
AVS(-) AT RL=10K			5,92	854.4	51	96.1	100.		4.00	00.0				10,	۸٠/٨
AVS(+) AT RL=2K			4.55	1.50	51	92.2	100		4.00	00.0	364.M.			105	^ ^ ^
AVS(+) AT RL=2K			878.M	631.4	51	98.0	98.0		00.4	0.00	-4.95			190	^ ^ ^
AVS AT 5V,-5V, PL=10K	1.95		7.19	1.31	21	98.0	98.0		2.00	0.00	3.96	0.00		1,0	۸٠/٨
AVS AT 5V,-5V, RL=2K	1.14		1.96	344.4	5	96.1	100.		2.00	00.0	-105.M			100	۸ / / ۸
SR(+) AT 16V,-16V			2.19	350.4	5	98.0	98.0		00.1	0.00	3,31			40.0	SO/A
SR(+) AT 16V,-16V	739.M		2.00	1.49	51	98.0	100		1.00	0.00	5.69			40.0	80/8
NOTES		FXCLUDE	S POPULA	TION OU	TSIDE (JF LOW	REJ AND HIGH REJ	HIGH	£.3						
	2./	X FAIL	* FAIL VALUES >OR= 5% ARE CIRCLED	0R= 5X	ARE CIR	SCLEU	:		;						
		FIGURE	DF MERIT	DEFINI	TIONS	L0-FM	LO-FM=(MEAN-LOW LIMIT)/SIGMA	LOW LIN	11)/816	¥.					
	/ 0	THE X F	THE X FAIL FOR ACT IS NOT VALID SINCE THE DUBL AND DIED DEVICES	2C 13	NOT VAL	TO OF	ALTERNATION CONTRACTOR OF THE DISA AND DISA D	4 1 1 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	217710	DEVICE	•				
		ARE COM	PARED TO	THE SI	NGLE	117			•						
	5./	THERE 1	THERE IS NO MAXIMUM FAIL LIMIT FOR GAIN AND SLEW RATE	IMUM FA	IL LIM	IT FOR	GAIN AN	D SLEW	RATE						

Table 4-8. Statistical summary of types 01, 02 & 03 at -55°C.

STATISTICAL CITA FOR ADEVICE	DEVICE	TYPES M	TYPES MIL/1119-01, 02	11, 02,	03 a	+125 DEĞREFS	REFS C		04 OCT	10	14:02:54				
PARAMETER	LOW	HIGH VAL EF	MEAN	SIGMA	SAMPLE SIZE	X IN 2	X IN 3	X FAIL	L04	L0.W	LO-EM	X FAIL	HIGH	HIGH	UNITS
•	1:	1.1	1./	1:	1.			2./			:	2./		ָרָ . י	
VIO(-C*) AT 2+,,-4V	-5.41	7.12	-615.	3.to	50	92.2	98.0	46	-7.00	-10.0	2.06	1.96	7.00	10.0	; ; ; ;
AT 28V	-5.40	6.64	-346.W	2.90	20	90.2	98.0			-10.0	5.29	1.96	7.00	10.0	> 2.
AT 158,-16V	-5.52	6.50	-472.W	2.96	20 10 10 10 10 10 10 10 10 10 10 10 10 10	2°26	98.0		-7.00	0.01	2.20	1.96	7.00	10.	7 :
VIO(004) AT 5/4-5V	-5.01	7.32	-281.K	2.90	ر د د	2.26	0.80	900	00.7-	0.01-	2.32	96.1	00.7	0.0	> <
V - 1/ - C TA	47.6 P	Y a	-943	2.43K	2.5	96.1	0.86		-20.0X	X0.04	7.83	00.0	×0.0	¥0.04	. e:
AT 29V	-10.6K	19.3K	-2.75K	5.12K	20	96.1	96.1		-30.0K	-40.0x	5,32	1.96	30 OK	40°04	A q
A7 16V16V	-8.02K	5.10K	-2.36K	2.70X	6 7	90°5			-20.0X	¥0.07-	6.54	3.92	20°0X	40.0X	۷d
AT = 24V	-17.2K	6.56K	-2.96×	4.12K	00 5	- de			-20°5X	20.04 20.04	2. 2.	96.0	20.04 5.04	. 0. 4 . 0. 4	Q 0
> 1000	-276.		7.10K	10.07	20	2000			10.0X	10.0K	. 6	90.0	, o	X	4 4
-	-7.65K	71.0K	14.7K	12.8K	3 5	96.1	98.0	000	10.0X	-10.0K	1.93		70.0Y	1101	. d
7	237.		19.7K	10.0K	20	94.1				-10.0x	2.96		70.0K	110.K	ρĄ
7	- 359.		10.0K	9.32K	47	88.2				-10.0K	2.15		70 °04	110.K	ρĄ
V	-500-		24.9K	12. 2K	5	94.1	98.0		10.0X	-10.0X	2.85		¥.001	110.K	~ :
-IIR(0C4) AT 16V-16V	-4.58X		16.0×	¥ ;	ر د د	94.1		96.0	. O. O.	¥0.0	82°		20°04	7. 2.	o
	82.0		7 P	000	~ 6	88.2	94.0	2 0	500	Y0.04	. 201		20°C	X 0 1	* &
VALUE IN TARGET	78.0		9.16	8.79	20	2.26 4.26		8	0	20.05	.32		× × ×	150.	a d
	58.0		94.6	10.3	51	96.1		- 8.	90.0	50.0	1.42		2.00K	150.	4
15v	-7.55		-6.11	1.19	5	98.0		00.0	-40.0	-100.	28.4		1.00K	0.00	4 1
-15v	0.00		5.20	1.38	2	96.1			-1.00×	0.00	72A.		40.0	100	₹
+VOP at Rust.	15.3		15.3	21.74	0 0	96.1				6 000	150.		200	16.0	> :
WOP AT PLOTIC	6.0		. 10.6	,	> (980		. 12.0	00.9	> :
17 dOA 17 dOA	59.0	7 ° 7	12.5	1.51	D C	100			1000		1.43	00.0	2002	. 6	> :
7 0 - 0	2007)		, <u>.</u>	0.00					424		3000		
. ~	25.0		4.73	1.14	2 2	94.1				000	527. W		105. X. X.		> > > >
A	0 40 M		3.29	2,17	51	100		(S)			326.W	00.0	105.K	100	\ \ \ \ \
	571.M		856.M	230,4	2	92.2					13.7	0.00	105.K	100	^^/^
	147.W		6.39	1.38	2	94.1		3,6	S.00		3.18	00.0	105.K	100	^:/^
٠ ا	147.1		C	405	~ ;	96.1	-	3	2°00		M 627	00.0	105.K	100.	> · · / > ·
-	5.00.	3.58	2.70	F . 659	<u>.</u>	96.1	c.	3.92	00.	00.0	2.58	0.00	20.0	40.0	SU/V
SR(+) AT 16:,-16V	2.000	6.25	4.58	1.31	21	96.1	98.0	3.92	.00		2.74	0.00	20.0	40.0	sn/A
NOTES:		XCL UDES	EXCLUDES POPULATION OUTSIDE OF LOW	LION OU	TSTDE (F LOW A	REJ AND	HIGH REJ	EJ						
	2./ 2	FAIL V	ALUES >	JR= 5%	ARE CIR	CLED									
		ICHAE O	F MERIT	DEFINI	11048:	L0-FW:	LO-FM=(MEAN-LOW LIMIT)/SIGMA	OW LIM	11)/816	¥.					
	4./ T	WE X FA	IL FOR	81 221	NOT VAL	TO SINC	D SINCE THE DUAL AND GUAD D	MIAL AN	7 7 7 16 T	AUAD DEVICES					
		0E COMP	ARE COMPARED TO THE SINGLE LIMIT	THE SI	VGLE LI	411									
	2.7	12 13 14 13	NO MAX	R L L	ור ויון:	ב ב ב	GAIN AND SLEA RATE	SLEA	RATE						

Table 4-9. Statistical summary of types 01, 02 & 03 at 125°C. 2.7

STATISTICAL DATA FOR ADEVICE TYPES MI	DEVICE	TYPES A	11./119-04, 05,	4, 05,	e 90	+25 DEGMEES	VEES C		03 OCT	79	15:06:20					
PARAMETER	LOW	H16H VALUE	ME A !!	SIGVA	SA 4PLE S17E	X 11: 2	1 11. 3 SIG"A		L1417	LOG	10-FW	X FAIL HIGH	H16H	HIGH REJ	HI-FM	UNITS
	1.1	1.1	1./	1.	1.			2./		; ;	1:	>. /		•	-	
VIO(-C4) AT 28V,-4V	-5.37	5.96	A3.37	2.29	•	95.1	100	•	-5.00	-10.0	2.15	1.23	5.00	10.0	2.22	 2
4	65.7-	4.60	-183.×	2,35	8	97.5	100			0.01-	50.5	0.00	5.00	10.0	2.20	> *
7	14. A.I	4.49	-248.M	2.37	.	α.	100			-10.0	1.98	0.00	5.00	10.0	2.23	>
A	-5.13	6.16	133.	2.34	a c 1	96.3		<u>~</u> (0.01-	5.19	15	5.00	10.0	2.0A	>
	-505-	504.	20.6	102.	7 1	3.00	91.	2		-300-	1.18	() ()	00-	300	778.M	A 4
	062	513	20.0	140	74	7.76	σ. α.	=		-600	2.56	3	300	009	1.72	P A
	-243	216.	7.47	83.0	7.5	25	C .)	00.	300	1.29		100	300	=:	ΡĀ
~	-20 H	27.8	21.7	83.4		C 6	٠ د د	₹ (*)	-100	300	- 46	<u></u>	-00	300	930° M	V d
>31124 A A A A A A A A A	456.	377	2 × 2 × 2	147	2 2	٠. د د د د د د	- a		-000-	.200	*		, oc	000	e	4 6
740-141	707	٠ م د م	41.0	• 00 •		· •		7 - 4	000		70.1		- 6	X	2.00	.
AT AV 24V	25.5	- K	161	144	2 2	200		7.47	000	500	2.7				C 2	4 4
AT 2AV, -4V	767	53.7	-148	130	5.	4 % to	97.5	6	-500	-500	402 M) =	200	0.04	2	. 4
442FV	57.6	1.94K	61A.	459	٦.	95.1	100	6	-500	-200	1.78	(2)	1.20x	2.50K	1.27	PA
_	110.11	281.	52.9	54.4	. R	8.8	φ. φ.	00.0	-500	.500	4.65		•u∙2	400	2.71	ρĀ
776-	21.5	300	194.	101.	67	80.2	90.1	00.0	-500-	-200	3.89	٩	540.	400	3.05	7 d
	0 7 8	124.	40.7	9.73	7.8	9.	96.3	0.00	80.0	0.09	2.02	00.0	2.00K	140.	195.	DA
	e :	124	95.8	10.5	18	91.4	00.	00.0	80.0	0.09	1.50	0.00	Š	140	182	80
	8	134	94.1	9.78	er e	K .	96.3	00.0	0.0	60.0	77.	0.0	7.00 X	140	195.	P. :
> :	- 20 -	6.0	-35.0	12.0	. .			00.0	0.08-	100	3.75	6.0	¥	0.0	86.2	4 : Y :
105(=) 4 154,=154	15.7	6.7	27.5	, v	, v	661		00.0	X00.	000	150		C .	.00	7.64	¥ .
	1 4 7			7 7 7 7	~						0 80				7070	۲ ۲ >
	9.9		2	90		9			200		75K				20 60	> >
RL=2K	13.4	7	14.2	5.82	. .	100		0.0	10.0	8.00	2.56	00.0	200	9.4	210	· >
	-14.2	-12.7	-13.6	655°4	 	100	100	00.0	-500	-16.0	285	00.0	-10.0	8.10	5,45	. >
4T PL=10K	72.7	1.26K		341.	75	92.7	95.6	0.00	50.0	0.00	1.35	2.47	¥.00	2.00K	291	٧٠./٧
AT RL=10K	70.6	1.60×		387.	2	94.0	B6.4	0.00	50.0	0.00	1.30	2.47	100.K	2.00K	257.	\ \ \ \
AT ML=2X	66.7	X0.4	356.	566	2 :	67.7	95.1		20.0	000	1.02	2.07	100 E	2.00K	333	> × ×
AVS AT 5V5V. R. 17.	6.7	1000 E	200	122	- C	٠ « ۲ «	. a) }	0.0	0	E 929	00.0	2.00	200×	527.	> ?
5V5V. RL = 2	411	800		132	90		01.				-		¥0.0	200	200	2 2 2 2
AT 16V,-16V	1.54	20.4		6.07	79	93.8	07.5	6	7.00	000	957.W	00.0	25.0	0.00	2.0	V/US
SR(-) AT 16V,-16V	1.44	23.8		5.20	91	93.R	100		7.00	0.00	1.21	0.0	25.0	40.0	2.26	N/US
NOTES:		EXCLUDES	ES PRPULATION OUTSIDE OF LO	110 VOI	301816	9F LO4	REJ AND	REJ AND HIGH REJ	Ĕ							
	~ ·	E FAIL VA	VALUES	OR= 5%	ARE CI	RCLED										
		FIGURE	•	DEFIN	19111) * 4 - 2 H	E COMPAN	HICKAN-LOW LIMITONOTOM HI LIMIT-MFANONOMA	TT)/SI(4 ¥						
	7.9	THE % F	AIL FOR	1CC 18	VOT VA	LID SIN	CE THE	FOR ICC IS NOT VALID SINCE THE DUAL AND GUAD	D QUAD	DEVICES	s					
		ARE COM	ARE COMPARED TO THE SINGLE LIVIT	THE S	INGLE	1411		•	1							
•	2.	THERE	S NO PARK	I FOR	אור רוא	IT FOR	GAIN AN	D SLEW	RATE							

Table 4-10. Statistical summary of types 04, 05 & 06 at 25°C.

STATISTICAL DATA FOR . FUICE TYPES MIL/119-04, 05, 06 8 -55')EGREES C	30173.÷	TYPES	/TL/119=	14, 05,	e 40	.55: 7£6!	SEES C		04 OC1	79 1	13:21:21				
PARAVETER	104 V4LUE 1.	HIGH VALUE 1./	WEAN.	\$164A	SA 4PLE \$12E 1./	X IN 2 SIGMA	X IN 3 SIGMA	x FAIL LOA 2./	L1411	LOW REJ	10-FM 3./ 1./	X FAIL HIGH P./	HIGH	HIGH REJ	UNITS
						:	!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!			;			!!!!	•	1 1 1
	-5.78	45.0		2.05	80	45.4	96.3	00.0	-7.00	-10.0		3.70 7.00	7.00	10.0	> 2
VIOC+CM) AT AV2AV	- B. 40	4.09		7.63	79	95.6	97.5	2.47	-7.00	-10.0		2.47	7.00	10.0	> 2
VID(0C4) AT 16V,-16.	. F. 36	9. A5		3.26	8.	93.8	97.5	2.47	-7.00	-10.0		3.70	7.00	10.0	> 2
VIOCOCH) AT SV,-SV	-5.51	9.52	70.44	3.03	11	88.9	95.6	0.00	-7.00	-10.0		(a)	7.00	10.0	> 14
+PSRR AT 8V,-16V	72.2	127.		9.41	£	91.4	100.	2.47	90.0	60.0		00.0	7.00X	140	0.0
-PSRR AT 16V,-BV	72.0	124.		9.83	٤.	95.1	100	5.47	90.0	60.0	1.55	0.00	2.00K	140.	, C
C4R AT 16V,-16V	65.0	120.		90.0	81	96.3	100.	4.94	A0.0	0.09		0.00	2.00K	140	33.
Ins(+) 4T 15V,-15v	9.05-	-21.4		9.00	8	100.	100	0.00	-80.0	-100.		00.0	1.00K	00.0	4 7
10S(+) AT 15V,-15V	3.15	51.5		10.A		97.5	100	0.00	-1.00K	0.00	95.9	00.0	A0.0	100	K.A
ICC AT 15V,-15V	2.07	8.57		1.66	7.8	95.1	100	:	!!!	2.00	1	61.9	73.50	10.0	4 >
+VOP AT PL=10K	14.6	15.1		100.4	8	96.3	100	00.0	12.0	8.00	24.1	6.0	200	16.0	>
-VOP AT RL#10K	-14.2	-13.9		126.4	79	97.5	97.5	00.0	-500-	-16.0	1.4AK	7.47	-12.0	-8.00	>
	A.70	14.8		1.00	÷	97.5	97.5	2.47	0.01	8.00	4.02	00.0	200.	16.0	>
	-14.0	-12.6		594.4	19	97.5	97.5	0.0	-500-	-16.0	314.	2.47	-10.0	-8.00	>
AVS(+) AT RL=10K	2.70	1.50X	492.	405.	89	82.7	94.0	2.47	25.0	00.0	1.16	00.0	105.K	2.00K	>:/>
AVS(+) AT RL=10K	15.3	1.20K	451.	382.	20	72.8	72.8	1.23	25.0	00.0	1.19	0.00	105.K	2.00K	^/
AVS(+) AT RL=2K	3.24	1.20K	337.	265.	7.3	87.7	R7.7	2.47	25.0	00.0	1.17	00.0	105.K	2.00x	\ \ \ \ \
AVS(-) AT PL=2K	0.80	1.41K	221.	259.	79	91.4	93.8	3.70	25.0	00.0	755.W	0.00	105.K	2.00K	^~/^
AVS AT 5V,-5V,RL=1	25.A	900	255.	193.	9,	67.7	93.8	0.00	10.0	0.00	1.27	00.0	105.K	2.00K	۸./۸
AVS AT 5V,-5V, RL = 24	16.7	800.	222.	232.	79	86.4	97.5	0.00	10.0	0.00	916.M	0.00	105.K	2.00K	1./1
SR(+) AT 16V,-16V	2.54	37.0	13.3	7.29	74	86.4	87.7	76	5.00	00.0	1.14	4.94	50.0	40.0	VIUS
SQ(+) AT 16V16V	1.31	32.3	13.9	6.21	81	91.4	100.	6. hg	5.00	00.0	1.44	00.0	50.0	40.0	N/US
NOTEN		FXCLUDE	S POPULA	1101 01	TSIDE	JF LOW	REJ AND HIGH	HIGH	P. J						
	2./	K FAIL	VALUES >	0R= 5X	ARE CI	SCLED			,						
		FTGUPE	FIGURE OF WEWIT DEFINITIONS: LO-FM	9EF1W	TIONS	LO-FM	LO-FM=(MEAN-LOW LIMIT)/SIGNA	LOW LT	417) / 51	Visit					
	7.0	THE X F.	TIME TO BE THE BOAT OF A THE BOAT AND BOAD DEVICES	1CC 18	NOT VAL	NIS OIT	CE THE .	PUAL AP	ON DOME	A DEVICES					
	•	ARE COM	PAGED TO	THE S	VGLE L	1171									
	2.1	THFRE T	S NO MAX	14 F(15)	ון רוש	IT FOK	CAIN AN	D SLEW	RATE						

Table 4-11. Statistical summary of types 04, 05 & 06 at -55°C.

) }					:								
PARAMETER	-01 -	HIGH	MEAN	SIGMA	SAMPLE	Z NI Z	X 1N 3			FO.	LO-FM	X FAIL	HIGH	н1Сн	UNITS
	12/	12/		1.1	812E 1./	SIGNA	SIGMA	ر دور	L 1 4 1 1	AE.J	M	H16H	L1411	REJ	
	!									;					
A	-7.60	A. R.B	102.4	•	11	91.4	93.8	6	-7.00	•10.0	2.68	1,23	7.00	10.0	>
VIO(+C4) AT 4V,-28V	-8.26	7.17	9A.1×	2,45	7.	41.4	93.R		-7.00	-10.0	2.90	1.23	7.00	10.0	>
VIO(054) AT 16V,-16V	-8.60	7.49	2.69.	2.52	11	91.4	93.A	6:19	-7.00	-10.0	2.78	1.23	7.00	10.0	> I
VIOCOCH) AT 5V5V	-8.94	7.2A	11.64	3.02	60	91.4	98°A	4.0	-7.00	-10.0	2.33	1.23	7.00	10.0	> 1
0-VID/D-T FROM 25 DC	-41.A		1.60	٠.	16	86.4	90.1	8.54	-30.0	-50.0	2.67	2.47	30.0	50.0	
110(-CM) AT 2AV,-4V	-5.04K	4.27K	-859.	2. 0.₹	<u>.</u>	93.A	100	0.0	-20.0X	-40.0K	9.52	0.00	20.0K	40.0k	PA
110(+CM) AT 4V,-24V	-19.6K	13.9K	-2.00K	5.44K	Ę	95.1	97.5	0.0	-30.0K	-40.0K	5.15	0.00	30°0%	40.04	
110(0C4) AT 16V,-16V	-21.AK		-1.41K	3.56K	Ë	97.5	98.8	1.23	-20.0K	10.04-	5.25	00.0	20.0K	40°0×	
110(+C4) AT AV,-24V	-22.4K		-1.7AK	4 0 0 K	£	93.8	98.8	1.23	-20.0K	-40.0K	3.69	00.0	20.0K	40.04	
Ā	-5.61x	23.7K	6.73K	6.91X	<u>.</u>	97.5	100	0.00	-10.0K	-10.0K	2.45	00.0	70.0X	110.K	Αq
4			19.9K	12. ex	3	97.5	100°	00.0	-10.0K	-10.0K	2,42	00.0	100.K	110.K	Ā
Ā			13.08	¥.0.	£	96.3	100	0.00	-10.0x	-10.0K	2.55	00.0	70.0K	110.K	PA
Ā	503°M		38.0K	11.3K	=	96.3	100	0.00	-10.0K	-10.0K	2.48	00.0	70.07	110.K	¥ d
	-5.72K		7.59K	7.46X	7	98.A	100	00.0	-10.0K	-10.0K	2.36	0.00	70.0K	110.K	4
-			21.9K	14.0K	æ	97.5	100	00.0	-10.04	-10.0K	2.28	00.0	100.K	110.K	Ā
	945		14.0K	10.18	81	5.16	100	00.0	-10.0K	-10.0K	2.41	00.0	70.0Y	110.K	4
-118(+C4) AT 8V,-24V	1.63×		19. AK	12,6K	~	98.8	100.	0.00	-10.0X	-10,0K	2,36		70.0K	110.K	Ā
+ PS&&	U 6 /	124.	101	9.57	7	91.4	97.5	1.23	A0.0	50.0	2.23		2.00K	150.	e O
	79.5	124.	98°	10.5	7.8	92.h	96.3	2.47	A0.0	50.0	1.73		2.00K	150.	e O
CAR AT 16V, -16V	. A1.4	124.	95.B	10.4	. 08	95.6	9. A.	0.00	30.0	50.0	1.51		2.00K	150.	р в
	150.0	-13.5	-30.9	15.8	7.8	96.3	100	00.0	-80.0	-100.	3.11		1.005	0.00	٩ ¥
IDS(-) AT 15V,-15V		30.1	18.	6.14	8.	100.	100	0.00	-1.00×	00.0	166.		80.0	100	Ā
ICC AT 15V,-15V	1.55	6.16	3.14	1.20	E	98.B ·	0 U S	!		00.0	-		3.00	10.0	۷ ¥
	14.9	15.3	15.1	104.4	7.8	95.1	96.3	3.70	12.0	A.00	29.4		260.	16.0	>
	-14.8	-14.4	-14.6	115.4	81	98.8	100	00.0	-500-	-16.0	1.62K		. 12.0	-8.00	>
+VOP AT RL=2K	13.2	14.9	10.1	9.44.4	7.8	96.3	96.3	3.70	10.0	8.00	6.42		200.	16.0	>
٦ ا	-14.3	-12.5	-13.6	760.4	æ	100.	100.	00.0	-500-	-16.0	245.		-10.0	-8.00	
*	50.7	1.20K	360.	263.	7	4° %	93.R	00.0	25.0	0.0	1.27		105.K	2.00K	
= !	34.3	1.20K	, A .	187.	6 1	96.3	96.3	00.0	25.0	0.00	1.36		105.K	2.00K	
AVS(+) AI KLEZA	0 7 7	1.50K	24 A	276.	7.3	82.7	86.4	e(25.0	00.0	806.M	00.0	105.K	2.00K	
:	8.70	1.20K	. H 9	141.	6/	46.3	96.3	€ }	25.0	٠ • •	453°M	0.00	×	7.00×	
- (50°4		148	-6		95.1	e.	0	19.0	0.00	1.16	0.00		2.00K	
<u>د</u> ا	21.1		116.	139.	ec 	95.1	97.5	ر د ا	c c	00.0	764.M	e.		7.0°2	
–	875.K	~	12.3	5.43	.	93.R	100.		5.00	0.00	1.34	0.00	e.	40.0	>
SR(-) AT 16V,-16V	1.90			4.34	8	95.1	100.		2.00	0.0	1.57	0.00		40.0	\$n/A
· Waten	•	90111120	4 11 000	200	10101	-	26.1 41.0	2							
•	_	Z FATI V	ALUES	08: 5	ARE CT	ביים ביים ביים ביים			3						
	×.	FIGURE OF MERIT DEFINITIONS: LO-FM=(MEAN-L	F MERIT	DEFINI	11048:	LO-FM	= (ME AN-	LO-FM=(MEAN-LOW LIMIT)/SIGMA	111)/51(AM.					
						HI-FWE(HI	:(H] L]	1, - 1 I y	1918/(NI	44					
	\	THE X FAIL FOR ICC IS NOT VALID SINCE THE	ITL FOR	100 18	VOT VA	LID SIM	3HE 30	DUAL AN	AND GUAD	GUAD DEVICES					
	,	ARE COMPARED TO THE	ARED TO	THES	VOLE L	- I									
	>•<	IMERE 18	X 4 10 10 10 10 10 10 10 10 10 10 10 10 10		ראור רוא	LIMII POR (A VIA	GAIN AND SLEW R	RATE						

Table 4-12. Statistical summary of types 04, 05 & 06 at 125°C.

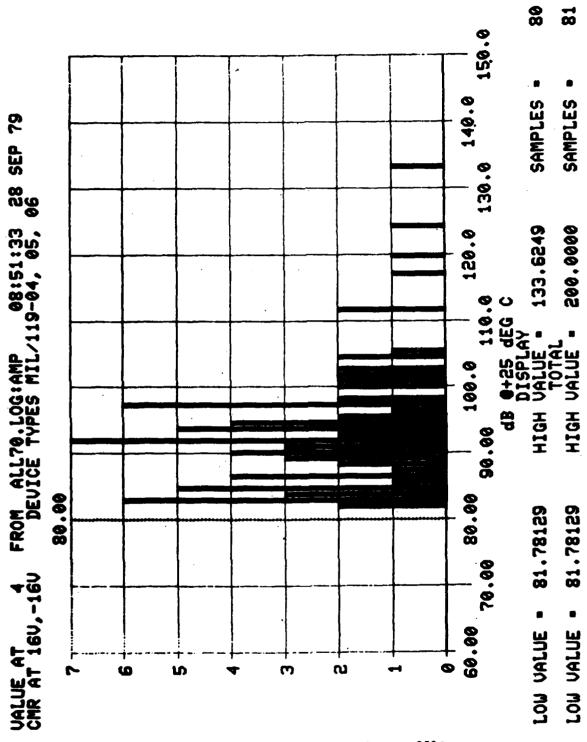


Figure 4-5. Common mode rejection at 25°C.

		Conditions $\pm V_{Cc} = \pm 15 \text{ V}$ (nargoranh 3 4 and Edgins 7 multiple				
Characteristics	Symbol	otherwise specified)	Devices	Min M	Max	linita
Input offset voltage	0I _A	= ± 5 V 0 V	ALL	-5	2	Λm
		$\pm V_{CC} = \pm 15V$ at $V_{CM} = \pm 11 V$, 0 V $-55^{\circ} C \le T_{A} \le +125^{\circ} C$	ALL	-7	7	Λω
Input offset voltage temperature sensitivity	AVIO AT	$\Lambda O = M^{2}\Lambda$	ALL	-30	30	ο «/ Λπ
Input offset	IIO3,	V_{CM} = 0 V L \le 25 ms $T_{\rm J}$ = 25°C	ALL	-100	100	bd
	1	TJ = 125°C	ALL	-20	20	Ąž
Input bias	+IIB		ALL	-200	1200	PA
		$V_{CM} = + 11v t \le 25ms$ $T_J = 125^{\circ}C$	ALL	-10	70	P.
	•IIB	T _J =	ALL	-200	200	b'd
	À1	$V_{CM} = 0 \text{ V}$, t $\le 25 \text{ms}$ $T_J = 125^{\circ} \text{C}$	ALL	-10	20	An
	77	ı	ALL	-400	200	ΡĄ
		$V_{CM} = -11V t \le 25ms$ $T_J = 125^{\circ}C$	ALL	-10	20	P.
Power supply	+PSRR	$+V_{CC} = 20V, 10V; -V_{CC} = -15V$	ALL	80		dB
rejection ratio	-PSRR	$+V_{CC} = 15V$; $-V_{CC} = -20V$, $-10V$	ALL	8		фB
Input voltage	CMR	4119 4 / 411	ALL	88		ф
rejection 4/		. OM S TT.				
1				_		_

See footnotes at end of table.

Table 4-13. Proposed MIL-M-38510/119 electrical characteristics.

	S.m.bo.1	Conditions ± V _{cc} = ± 15 V (paragraph 3.4 and Figure 7, unless	<u></u>	Limits	t s	
	эушрог	ornerwise specified)	Devices	Min	Мах	Units
Adjustment for input offset voltage	V _{IO} ADJ (+)		01, 02, 04, 05	φ		Λ̈́E
77	V _{IO} ADJ (-)		01, 02, 04, 05	,	8-	À
Output short cir-	•	,	01,02,03	-40	•	¥
positive output) $\frac{5}{2}$	+0s(+)	t 🗲 25 mS (Short circuit to ground)	04,05,06	-80	•	
Output short cir-			01,02,03		07	1
cuit current (for negative output) $\frac{5}{}$	(-) so ₁	t \$ 25 mS (Short circuit to ground)	04,05,06	ı	80	€
Supply current	DOI	TA = 45°C	01,02,03		0.3	-
(per amplifier)			04,02,06	-	3.5	<u> </u>
		25°C < TA < 125°C	c 01,02,03	•	0.3	-
			04,05,06	•	3	
Output voltage	+ VOP +	$R_{\rm L} = 10~{\rm K}$ A.	ALL	±12.5	•	>
Swing (maximum)	VOP	RL = 2 KA	04,05,06 ±11	117	1	
Open loop voltage	Avs (+) ,	$V_{out} = \pm 10 \text{ V}$ $T_{A} = 25^{\circ}\text{C}$	01,02,03	5		/
(papua argurs) urag	AVS (-)	= 10 K	04,05,06	50	•	AII / A
િ		04-06, R _L = 2 K -55°C < T _A < +125°C	01,02,03	7		
			04,05,06	25	-	
Open loop voltage	Avs	$\pm v_{CC} = \pm 5 v$	01,02,03	3		
/9 (single ended)		$R_L = 10 K_A$ $V_{out} = \pm 2V$	04,05,06	10	•	Λ II / Λ•
			7			

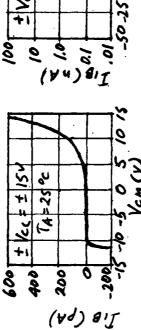
Table 4-13. Proposed MIL-M-38510/119 electrical characteristics (cont.).

Characteristics	Symbol	Conditions $\pm V_{CC} = \pm 15 \text{ V}$ (paragraph 3.4 and figure 7, unless otherwise specified)	= ± 15 V figure 7, unless d)	Device	Limita Min M	Max	Units
Transient response Rise time	TR(tr)	$v_{IN} \approx 50 \text{ mV}, A_{V} = 1$ $c_{L} = 100 \text{ pF}$	$\frac{R_L = 10 \text{ K} \Omega}{R_L = 2 \text{ K} \Omega}$	01,02,03	- 4(700 700 700	ns
Transient response Overshoot	TR(os)	See Figure 8	$R_{\rm L} = 10 \text{ Kg}$ $R_{\rm L} = 2 \text{ Kg}$	01,02,03		2 03	%
Slew rate	SR (+) and	VIN = ± 5 V	п	01,02,03	2 7		V/us
	SR(-)	AV = 1 see Figure 8	TA = -55°C, 125°C	01,02,03 04,05,06	5	[.].	
Settling time	ts (+) and ts (-)	(0.1% error) $T_{A} = 25^{\circ}C$ see Figure 9	AV = 1	01,02,03 04,05,06	- 6000	88	ns
Noise (referred to input) broad- band	N _I (BB)	Bandwidth = 10 kHz see Figure 10	T _A = 25°C	ALL		15	uVrms
Noise (referred to input) popcorn	N _I (PC)		T _A = 25°C	ALL		80	uVpk
Channel separation	. SD	see Figure 11	$T_{A} = 25^{\circ}C$	02,03,05, 06	80		dB

Table 4-13. Proposed MIL-M-38510/119 electrical characteristics (cont'd).

NOTES:

- increase in junction temperature T.1. Measurement of bias current is specified at T.J rather than Bias currents are actually junction leakage currents which double (approximately) for each 10°C IA, since normal warmup thermal transients will affect the bias currents. The measurements for Measurement at T_A = -55°C is not necessary since expected values are too small for typical test bias currents must be made within 25 ms after power is first applied to the device for test. 7
- Bias current is sensitive to power supply voltage, common mode voltage and temperature as shown by the following typical curves: 7



- $\frac{3}{1}$ In is calculated as the difference between + IIB and IIB.
- $\frac{4}{4}$ CMR is calculated from VIO measurements at V_{CM} = + 11V and 11V.
- Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that T_J (max) < 175°C. 5/
- Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents. ۱و
- Offset adjustment pins do not exist for 8 pin dual and 14 pin quad packages.
- Channel separation is only applicable for the dual and quad devices. ø۱

Table 4-13. Proposed MIL-M-38510/119 electrical characteristics (cont'd).

SECTION V

12 BIT A/D CONVERTER

Table of Contents

		Page
5.1	Background and Introduction	v-1
5.2	Description of Device Type	V-2
5.3	Characterization of the 5200 and 5210 Series A/D Converters	V-6
5.3.1	Static Test Parameters	V-6
5.3.2	Static Test Circuit	v- ₁₀
5.3.3	Devices Used For Testing	-
5.4	Automatic Test Development	V- 19
5.4.1	Test Program Development	V- 20

LIST OF FIGURES

Figure	No Title	Page
5.1	Approximate schematic of 5200 A/D Converter with external reference	4
5.2	Timing diagram of the 5200 series A/D Converter	5
5.3	Block Diagram, 12 Bit A/D Converter Test Circuit	11
5.4	Static Test Circuit	12
5.5	Reference Module Schematic	13
5.6	Simplified Interconnect Schematic	16
5.7	ADC input voltage vs time when measuring 0110 to 0111 transition voltage	17
5.8	ADC input voltage vs time when measuring 0111 to 1000 transition voltage	18
	LIST OF TABLE	
No.	Title Title	Page
5.1	Device Specification	8
5.2	Abbreviated Test = "A "address input codes	2/

SECTION V

CHARACTERIZATION OF 12-BIT A/D CONVERTERS

MIL-M-38510/120

5.1 Background and Introduction

This JAN 38510 specification development for A/D converters is new in at least two respects: it is the first slash sheet devoted to A/D converters, and the specified devices are the first linear hybrids to be designated for military usage in the JAN program. The need for data converters in military systems is well-established, not only for new microprocessors-based digital systems, but for retrofit into upgraded existing systems. For example, a system using resolvers to transmit angular position/rate data to other analog computing subsystems may be upgraded by retaining the sensing resolvers, converting their outputs to digital numbers, and replacing the analog computing subsystems with digital counterparts. High-resolution, high accuracy converters would be required to accommodate the wide dynamic range and typical system accuracy required.

At this time, high speed (e.g. 13 to 50 usec conversion time) 12-bit A/D converters do not exist as monolithic devices, although lower speed and/or lower resolution monolithics are becoming available from several manufacturers. The hybrid devices selected for this slash sheet are already used in numerous military systems. They were developed by Micro Networks Corporation, and at least some of the device types will also be available from other hybrid manufacturers ... Analog Devices and Hybrid Systems. Generally, the devices offer choice of external or internal references, two conversion times, and four input voltage ranges.

There is valid concern amongst all device manufacturers regarding the required testing of A/D converters. Test capabilities may range from bench tests, to custom test boxes, to fully automatic test systems. At GE, two levels of test were planned ... both a bench test and a fully automatic test using the Tektronix \$3260 system. Admittedly, the latter system is not used by any manufacturer, but GE's test development has a dual purpose ... to verify the test circuit and to characterize the device. Since both D/A and A/D test developments were proceeding in parallel, a common precision reference D/A section was developed to share with both test adapters. The test circuit recommended for the slash sheet should be compatible with a variety of automatic test systems. Deviations from the test circuit are permitted but must be justified by the manufacturer at the time of qualification submittal.

Test philosophy regarding linearity and monotonicity is another controversial subject. One manufacturer verifies linearity by measuring deviations from a best-fit straight line, while another measures deviations from a line connecting end points. Since users cannot calibrate to some unknown best-fit line, but can calibrate to full-scale end points, GE strongly favors the latter method. (There is further discussion on these topics within the text.)

At this report tine, the A/D characterization effort is not yet complete. A slash sheet has been prepared in preliminary status, and has been issued to interested people for comment. Test philosophy has been established, and test circuits and adapters were designed and fabricated for both bench testing and Tektronix S3260 testing. Test software has been developed and has been debugged. The remaining effort to complete the characterization is to complete the data taking, analyze the data, recommend changes (if any) for the slash sheet, issue the data, and finalize the slash sheet.

5.2 Description of Device Types

There are two series of device types included in /120, the Micro Networks MN5200 series and the MN 5210 series. In each series there are eight device types, four pair having input voltage ranges of 0 to -10V, -5V to +5V, -10V to +10V, 0 to +10V, with each pair having either an internal or an external reference. Both series are 12-bit successive-approximation converters having both serial and parallel digital outputs. They are packaged in miniature 24-pin glass/ceramic DIPs, are self-contained and internally laser-trimmed (no external adjustments). The two series differ only in maximum conversion time ... the 5200 series (device types 01-08) requiring 50 usec max for a complete conversion, and the 5210 series (device types 09-16) requiring 13 usec max.

The hybrid devices have several chips; there are significant differences in the number of chips used by different manufacturers. Basically, the successive approximation converter consists of a D/A converter (ladder network and switches), a successive approximation register and logic, and a comparator. An approximate diagram of the 5200 A/D converter is shown in Figure 5-1, which includes functional level information only, not detailed schematics of all sections. The 12-bit converter must make 12 successive approximations of the applied input voltage. While this is occurring, the input cannot change (unless it were to change so as not to affect previous trials, which is too restrictive), so a sample/ hold circuit is normally used to hold the input constant during the conversion time. The 12 comparisons are made between the input voltage and a feedback voltage obtained from the internal 12-bit parallel D/A converter, beginning first with the MSB and ending with the LSB. The comparator output determines whether a "1" or a "0" should be entered in the register for each bit comparison. In the figure, this function is performed with a high-gain precision comparator A2.

The 25L04 successive approximation register contains most of the digital control and storage necessary to operate the converter. It contains a set of master latches acting as control elements which change state when the external clock input is low, and a set of slave latches that hold the register data and change state on a low-high transition of the input clock. It acts as a serial-to-parallel converter for information from the comparator A_2 , sending it to the appropriate slave latch to appear at the register output (serial output) when the clock transition goes from low-to-high. When that data enters the register, the next less significant bit is set to a low, ready for the next iteration.

A timing diagram is shown in Figure 5-2. For parallel data outputs, the shaded areas shown denote states determined by data input immediately prior to the shaded area. Parallel data is valid for the entire time that the EOC signal is low, i.e., until the converter is reset. The converter is reset by holding the "start" signal low during a low-to-high transition of the clock, beginning at least 25 nsec prior to the clock transition. When the start is again set high, the conversion will begin on the next low-to-high clock transition. The start signal can be set low at any time during a conversion and it will reset the converter. A complete conversion takes place in 13 clock pulses. For continuous operation, the user has to connect "start convert" to EOC, pin 1 to pin 22. The ground terminals must be externally connected together as close as possible to the device.

Op Amp A₁ buffers the input reference voltage and in conjunction with transistor Q14 provides the base line voltage to all switching transistors. The base line voltage varies to compensate for the variation in the switching transistor V_{BE} 's with temperature, thereby providing a constant voltage to the ladder resistors. Similar compensation exists for variations in the minus supply voltage, which would change ladder currents.

It should be noted that the 5210 series of devices manufactured by Micro Networks require a 2.2 uF solid tantalum capacitor connected between DUT pins 15 and 10 for operation with conversion times of 24 usecs or less.

The user should be aware that there are differences in the supply currents among vendors, and also differences in power supply sensitivity. The specification tolerances have essentially been widened to accommodate both vendors. Proper system design considerations by the user will permit interchangeability by using the specified limits. Tighter performance may be obtained from a single vendor on power supply sensitivity, but this is not guaranteed or controlled within the spec, except as stated.

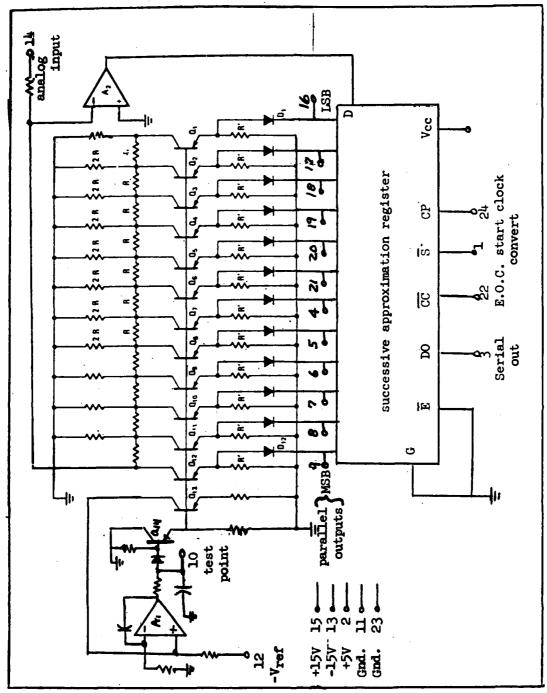


Figure 5-1. Approximate schematic of MN5200 A/D Converter with external reference.

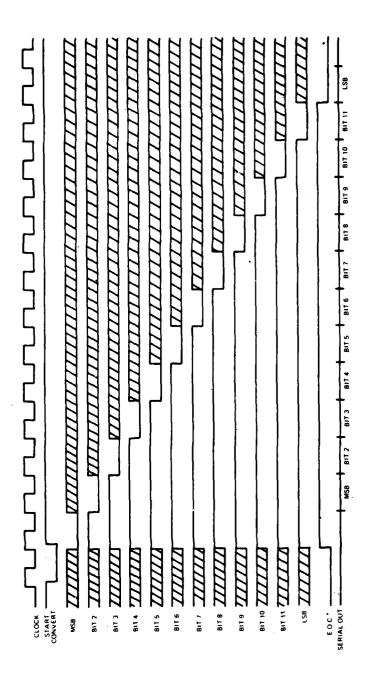


Figure 5-2. Timing Diagram for the 5200 series A/D Converter

5.3 Characterization of the 5200 and 5210 Series A/D Converters

5.3.1 Static Test Parameters

Power Supply Currents

Power supply currents limits have been enlarged to encompass all device manufacturers designs since no two devices are implemented identically. Each must, however, satisfy the maximum power dissipation requirements.

Power Dissipation

The device power dissipation is the sum total of the products of the power supply currents and their respective voltages plus, for devices with external reference voltage only, the product of the reference input current and voltage.

$$P_D = V_{cc} I_{cc} + V_{EE} I_{EE} + I_{LOG} + \underbrace{V_{REF} I_{REF}}_{\text{(EXT REF. ONLY)}}$$

Input Logic Voltage Levels

Logic "1" input voltage levels is + 2 V minimum and Logic "0" input voltage levels is + .8 V maximum, typical digital logic levels. Inputs are: S.C. and Clock.

Output Logic Voltage Levels

Output logic "1" voltage is 2.4 V minimum when loaded with 320 uA (source). Output logic "0" voltage is 0.4 V maximum loaded with 3.2 mA (sink). Outputs are: 12 address outputs; E.O.C; and SDO.

Output Short Circuit Current

All outputs are tested with a short circuit applied. Output current shall not exceed - 25 mA.

Input Low Current

Input low current is the maximum sink current the device will sink with the input at 0 V_{\bullet}

Input High Current

Input high current is the maximum current the device will source with the input voltage at + 5 V.

Input Impedance

The specification calls for input impedance measurement. On the S3260 a dc resistance will be measured.

Clock Input Pulse Width

Clock input pulse width is specified as 200 ns. The positive portion of the clock pulse (logic 1) must be equal to α greater than 200 ns wide for all device types.

Minimum Conversion Time

Minimum conversion time is a function of the speed of the converter and limits specified are maximum values. The maximum value of minimum conversion time represents the maximum conversion speed the device must be capable of at rated accuracy.

Power Supply Sensitivity

Power supply sensitivity is specified as the percent of full scale voltage range change per percent change in power supply voltage.

Zero Error

For a unipolar device the straight line between the first and last transition voltage is extended beyond the first transition voltage 1/2 LSB. The difference between the resulting voltage and zero volts is unipolar zero error.

For a bipolar device add 1/2 LSB to the transition voltage for the 0111 1111 to 1000 0000 0000 transition and difference between the resulting voltage and zero volts is the bipolar zero error. If "Best Fit Linearity" is employed the offset employed to shift the curve will have to be factored into the zero errors, unipolar and bipolar.

Absolute Accuracy

Absolute accuracy is accuracy with which the A/D converter will measure and convert an analog voltage to a digital equivalent, relative to an accurate voltage standard. Quantization error is reduced to \pm 1/2 LSB by offsetting the transition voltages by 1/2 LSB.

Table 5.1 Device Specifications

			- 1		
			Device Type	Types 01 - 13	
Characterizations	Symbol	Conditions/Remarks	MIN	MAX	Units
Power Supply Current from V _{CC}	$^{ m D}_{ m I}$		3	28	МА
Power Supply Current from V _{EE}	IEE		-35	-1	шA
Power Supply Current from V _{1,0G}	$_{ m ILoc}$		1	42	шA
Power	Ę	Device Types - 02, 04, 06, 08, 10, 12, 16 Device Types - 01, 03, 05, 07, 09, 11, 13, 15		0.8	3 3
Ref. Input	IREF	Exter 8, 10	0.1	2	тА
Input Logic Voltage Levels Logic "1" Logic "0"	TI A		2	8.0	> >
Output Logic Voltage Levels Logic "1" Logic "0"	HO _A	I _L = 320 uA I _L = 3.2 mA	2.4	0.4	> >
Output Short Circuit Current	OSO _I	$T_{A} = +25^{\circ}C, V_{IN} = +10.5 V$	-25	0	μA
Input Low Current	$_{ m II}$	$V_{IN} = 0 V$		9*-	mA

Table 5.1 Device Specifications (Cont.)

			Device Types	es 01 - 13	
***************************************	C.m.b.o.1			Limits	
Cilatar tel 12a (10ils	Symbol	Conditions/Remarks	MIN	MAX	Units
Input High Current	LIH	$V_{IN} = + 5 V$		07	ηγ
Input Impedance	$_{\rm I_2}$	Device Types - 01 to 04, 07 to 12,			
	1	15, 16 Device Types - 05, 06, 13, 14	3.5	10	ችች
Clock Input Pulse Width	CPW		200		su
Minimum Conversion Time	£°CI	Device Types - 01-08 Device Types - 09-16		50	sn sn
Power Supply Sensitivity VCC	PSS1	Device Types - 01,03,05,07,09,11,13,15 Device Types - 02,04,06,08,10,12,14,16		±.02 ±.02	%FSR/ %P.S.
Power Supply Sensitivity VEE	PSS2	Device Types - 01,03,05,07,09,11,13,15 Device Types - 02,04,06,08,10,12,14,16		±.05 ±.02	%FSR/ %P.S.
Resolution		The device shall exhibit no missing codes		12	BITS
Zero Error		${}^{V}_{CC} = + 15 \text{ V} \pm .015 \text{ V}$ ${}^{V}_{EE} = -15 \text{ V} \pm .015 \text{ V}$		2	LSB
Absolute Accuracy	·	${}^{V}CC = + 15 \text{ V} \pm .015 \text{ V}$ Ext. Ref. ${}^{V}EE = -15 \text{ V} \pm .015 \text{ V}$ Int. Ref.		+ + 1	%FSVR
Integral Linearity Error		$^{\text{VCC}}$ = + 15 V \pm .015 V $^{\text{VEE}}$ = - 15 V \pm .015 V		±1/2	LSB
Major Carry Errors	MCI -	4000 - 377 (Octa) to 2 - 1 Relative to REF DAC Major Transition Voltage		+1	LSB

Integral Linearity Error

Integral linearity is the deviation from the ideal linearity curve (a straight line). The ideal linearity curve would be a straight line between the first and last transition voltages if linearity was specified as "Ind Point". If, however, "Best Fit Linearity" is employed, linearity is the deviation from the "Best Fit" straight line.

Major Carry Errors

Major Carry Errors are a measure of the differential non-linearity of the A/D converter. If major carry errors are less than : 1 LSB and the device is linear, there will be no missing codes.

5.3.2 Static Test Circuit

The circuitry used to test the MN5200 series of A/D converters is shown in Figures 4 and 5. Figure 5.3 shows a simplified block diagram of the schematic. The transition to be tested - l LSB is entered into the A_n register, where it is applied to the reference DAC and a digital comparator. The digital comparator's other input comes from the device under test, a 12 bit A/D converter. The latch inserted between the ADC and the digital comparator insures that only valid data is applied to the comparators, i.e. it is strobed when an end of convert signal is received from the ADC.

The digital comparator has 3 possible outputs, $A \angle B$, A=B, or A > B depending on the relative magnitude of the transition to be tested and the present state of the A/D converter. If $A\angle B$, the input to an integrator is connected to + 5 volts through an analog switch. This causes the integrator to ramp downwards. The output of the integrator is summed with the analog output of the reference DAC. Since the DAC output is a constant DC level and the integrator's output is decreasing their inverted sum is rising, which forms the analog input to the ADC. The ADC's input voltage will continue to increase and its digital output word will continue to decrease until the digital comparator decides that A=B or A > B. When this happens, the analog switch changes state, connecting -5 volts to the input of the integrator. This causes the output of the integrator to ramp upwards. When summed with the DAC output, this forces the ADC input voltage to decrease, which increases its digital output word.

In this way it can be seen that the ADC digital output word locks onto the word present in the A_n register, and couples between $A \leftarrow B$ and A = B.

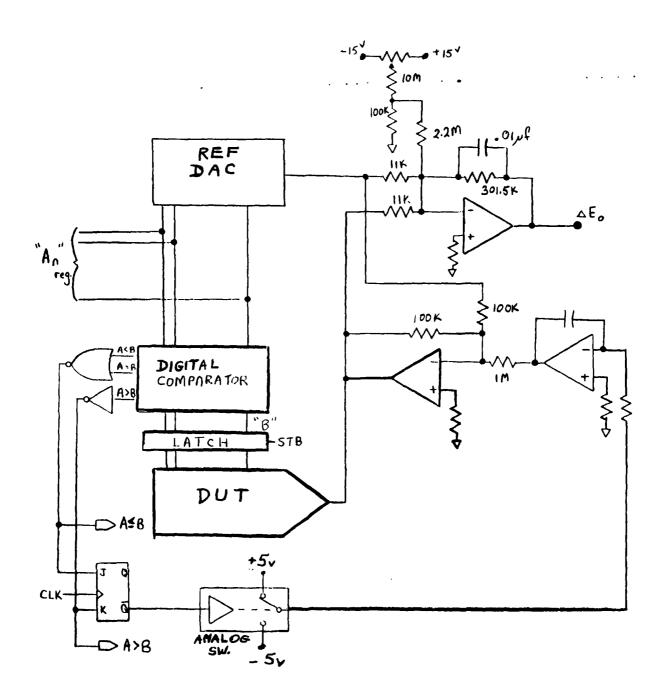


Figure 5.3. Block diagram, 12 Bit A/D Converter test circuit.

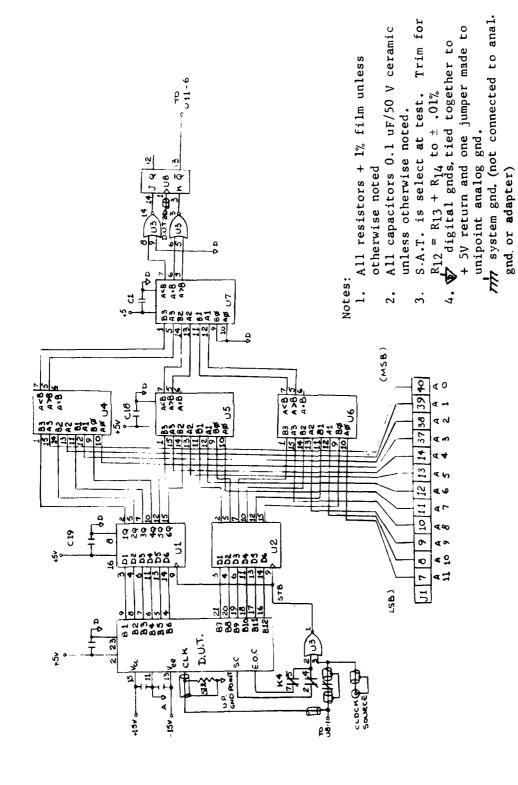


Figure 5.4. Static Test Circuit. (cont'd next page)

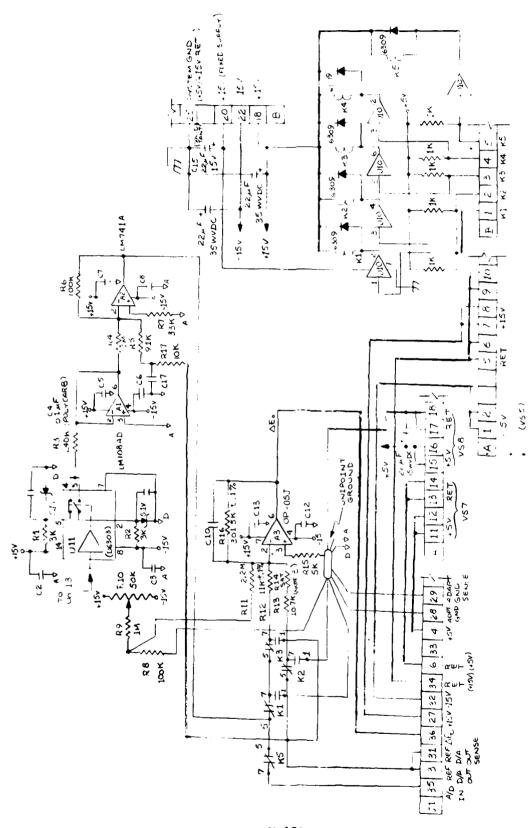
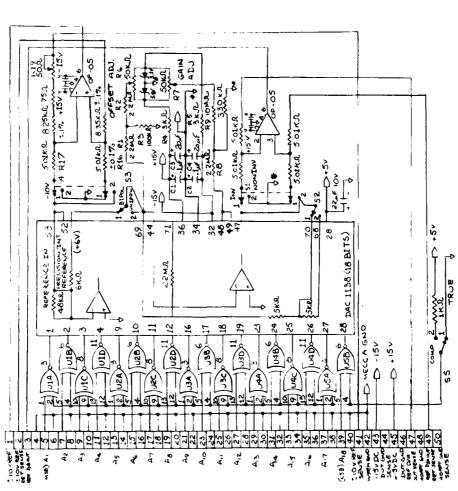


Figure 5.4. Static Test Circuit. (cont'd)

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1 for unipolar 6.
-5v range
-5v range
2 for -10v range
1 for bipolar
operation
2 for unipolar
operation
2 for +10v Ref

S3

\$4 낆

\$2 \$3

2 for comp logic

volt

For use in conjunction with the 12 bit A/D converter S3260 Test Adapter S1 in position 1 (Inv) for

5

Notes:
1. For use in conjunction with the 12 bit D/A converter \$3260 Test

Adapter Sl in position 2 (Non Inv) S2 " l for unipol

MNS200 - MNS205 MNS210 - MNS215 for MNS200,

MN5206, MN5207 MN5216, MN5217

2 (Non Inv) for

S

22

MN5210, MN5211, MN5213, MN5214,

MN5204

MN5203, MN5201,

MN5211, MN5212, MN5214, MN5200 MN5203, MN5206,

23

MN5207, MN5210 MN5213, MN5216

l for -10v Ref. Volt

MN5217

1 for MN5206,

\$5

%

MN5202,

MN5205

\$2

Reference module schematic. Figure 5-5.

THIS PAGE IS BROT QUADITY PRACTICABLE ביני טון ישבוני בינבר זו א זיט אנאאון The output of the reference DAC and the analog input to the ADC are summed in the error amplifier. A potentiometer is used to null the offset of this amplifier to zero. The capacitor in the feedback loop tends to average out the fluctuations in the A/D input voltage due to the ramping effect of the integrator. The ADC transition voltage can be calculated by dividing \triangle $E_{\rm O}$ by the gain of the error amplifier, and then subtracting the reference DAC voltage.

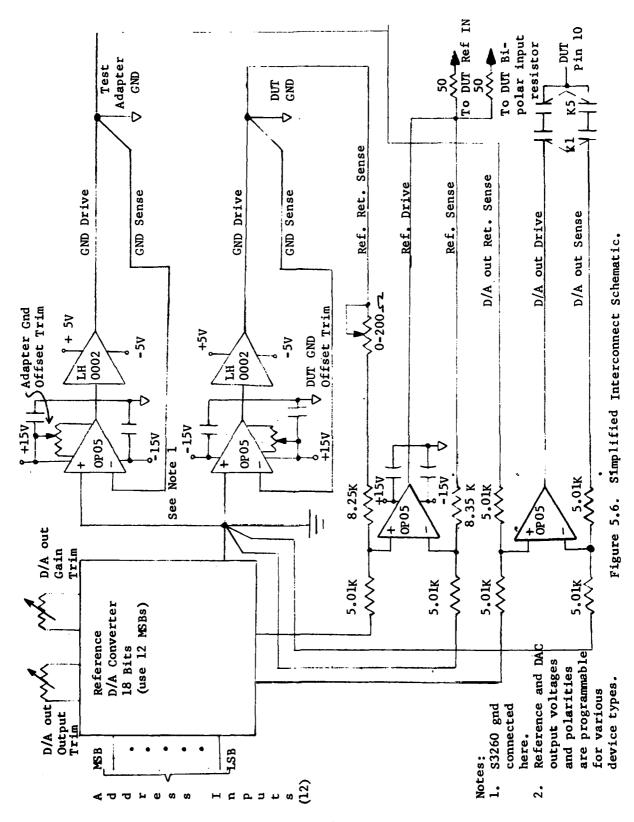
Figure 5.7 shows the ADC input voltage vs time when the transition voltage from 0110 to 0111 is to be measured. It is assumed that the ADC performs a conversion every 10 usec and the analog input to the A/D converter ramps up or down at a rate of .005 LSB/usec. When conversion #1 is complete, the reference DAC input (0110) is equal to the ADC output so the integrator continues to ramp upward. The same thing is true when conversion #2 is completed, 10 usec later. When conversion #3 is complete, however, the ADC output is greater than the DAC input, so that A B and the integrator begins to ramp downward. The ADC input voltage will continue to cycle around the transition voltage from this point onward. It should be noted that in Figures 5.7 & 5.8 downward refers to increasing, and upward decreasing ./D input voltage.

In the previous example the maximum difference between the actual transition voltage and the input to the ADC at any time was .05 LSB. In measuring some transitions this difference may become as large as .1 LSB due to the way in which the ADC performs conversions. Because the MN5200 series of ADC's are successive approximation devices they perform conversions by setting one bit at a time, starting with the MSB. Figure 5.8 shows the ADC input voltage vs time when measuring the 0111 to 1000 transition voltage. After conversion #1 is completed the ADC input voltage will ramp upwards because A=B. The same thing is true when conversion #2 is completed 10 usec later. Conversion #3 is now begun, starting with the MSB. Because the analog input to the ADC immediately following conversion #2 is still less than 1000, the MSB will be set to a O. The remainder of the bits will be set to 1, resulting in an ADC output of 0111 at the end of conversion #3. Since this is still equal to the input to the DAC, the integrator continues to ramp upwards. Conversion #4 will result in a value of 1000, and the integrator will begin to ramp downwards. Conversion #5 also results in a value of 1000, and the integrator continues downward. Conversion 6 is now begun, starting with the MSB. Because the input to the ADC immediately following conversion #5 is still greater than 1000, the MSB will be set to a 1. The remainder of the bits will be set to 0, resulting in an ADC output of 1000 at the end of conversion #6. Since this is still greater than the input to the DAC, the integrator continues to ramp downwards.

The ADC input will continue to cycle around the transition voltage from this point onward. The reason that the ADC input voltage did not stray as far from the actual transition voltage when measuring the 0110 to 0111 transition was that in that case only the least significant bit was changing, which is the last to be set in a conversion. In both cases the sawtooth around the actual transition voltage is filtered out in the error amplifier by a capacitor in the feedback loop.

5.3.3 Devices Used For Testing

(later)



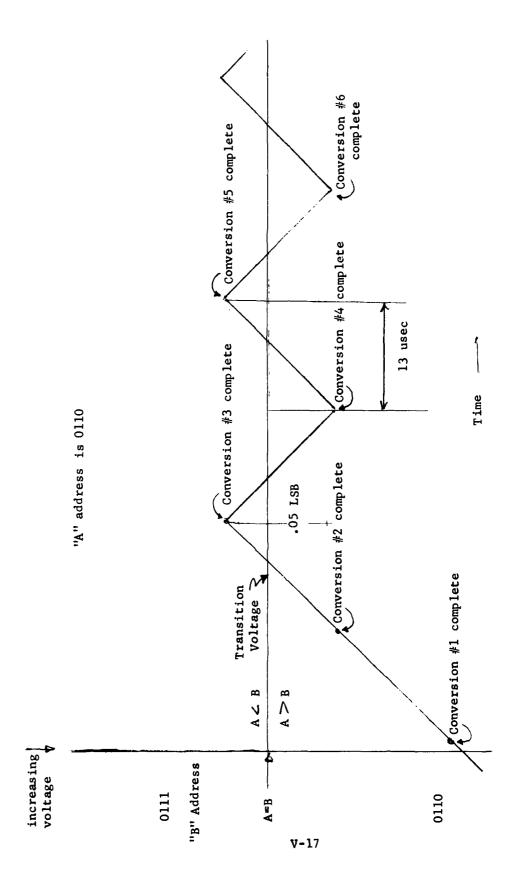


Figure 5.7. ADC input voltage vs time when measuring 0110 to 0111 transition voltage.

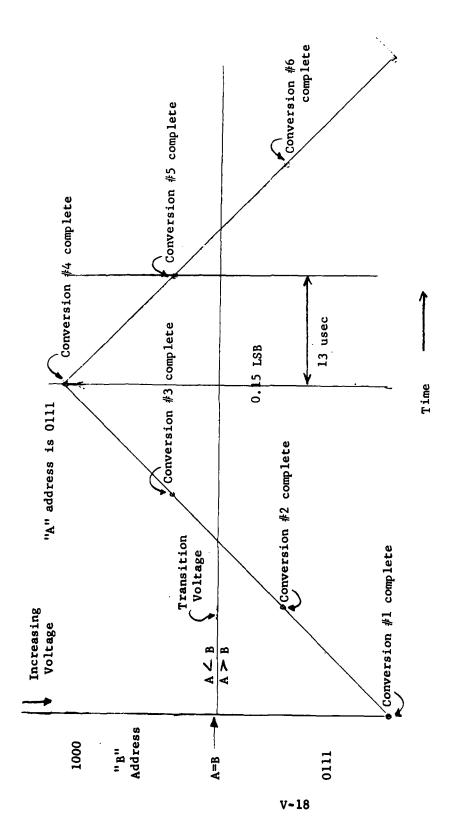


Figure 5.8. ADC input voltage vs time when measuring 0111 to 1000 transition voltage.

5.4 Automatic Test Development

Testing A/D converters, particularly 12 bits or more, is a difficult task and is generally only performed by the most sophistocated of the users. Traditionally, A/D converters were tested using a D/A converter in conjuction with an oscilloscope. The D/A converter generally had at least 4 bits more than the device to be tested. The implementation varied but in all cases the testing was tedious, time consuming, and required human data logging. Manufacturers of the devices, in an effort to reduce test time and costs, are attempting to automate the testing of A/D converters. Some already have.

A major portion of this characterization effort was devoted to the development of an automatic test capability for the S3260.

Once the decision was made to test A/D converters automatically, the next decision to be made was how to implement the testing. Did all transitions have to be tested or could an abbreviated test method be employed which tests bit errors and utilizes superposition to test the worst case linearity? Unlike the D/A converters for which the abbreviated test method has been used successfully by most manufacturers, the A/D converter transition voltages are not so clearly defined. A/D converters are tested at maximum rated speed which results in transient errors that will distort static bit weight errors. One of the objectives of the 5200 characterization effort will be to determine whether or not an abbreviated test method could be employed with sufficient confidence that devices with missing codes would be detected. It should be noted that when testing A/D converters, transition voltages are measured and not dc voltage levels. Transition voltages are nominally set at 1/2 LSB below nominal voltage levels to reduce quantization errors to ± 1/2 LSB.

Linearity is, without a doubt, the most difficult A/D converter parameter to measure accurately and unless clearly defined may confuse the user. Some vendors choose to use "Best Fit Linearity" as opposed to "End Point Linearity". One could argue that "Best Fit Linearity" would be achieved by utilizing a Least Squares Straight Line but that would most certainly confound the less sophistocated user. GE would prefer to utilize "End Point Linearity" but, since high speed successive approximation A/D converters are not necessarily linear, "Best Fit Linearity" will be employed. "Best Fit Linearity" will be defined as the straight line parallel to the "End Point Linearity" straight line that distributes maximum positive and negative linearity errors equidistantly from it. This is a definition that the user can easily comprehend and apply.

To make the testing of a 12 bit A/D converter accurate utilizing a Tektronix S3260, it was necessary to design a reference module which contains an 18 bit reference DAC, buffer, active ground drives, and switching to provide the proper voltages and logic levels to test all of the device types in the slash sheet. Since the characterization efforts for the 562, 12 bit D/A converter, was performed concurrently with the 5200 series A/D converters, the reference module was designed to accommodate both testers. The reference module, in conjunction with the S3260 test adapter, can be utilized on the bench if the S3260 undersocket connections, power supplies and relay actuators, are implemented in the bench setup. Manual addressing of the reference DAC is provided via toggle switches. Display of the DUT output address can be accomplished by connecting a buffered 12 bit LED display to the DUT output address register via a pair of DIP clips.

The technique employed to measure transition voltage employs a dither which ramps slowly above and below the transition voltage. A more detailed description of the test circuit is contained within the text of this report. Part of the test development will be to select the proper dither voltage for the devices being tested. Too low a dither voltage and it will be down in the noise level. Too high a dither voltage and it will limit the range of differential non-linearity measurement. A finite amount of dither will provide some guard banding for detecting devices that might marginally exhibit missing codes.

5.4.1 Test Program Development

Software was developed for the Tektronix S3260 test system to provide for automatic testing of the MN5200 series of Analog-to-Digital converters. The test circuit used in conjunction with the S3260 is shown in Figures 5.4, 5.5 and 5.6.

Power Supply Currents

Supply currents are measured first with all bits off and then again with all bits on. + 15 VDC is forced on pin 15 and the current flow, $I_{\rm CC}$, is measured. + 5 VDC is forced on pin 2 and the current flow, $I_{\rm LOG}$, is measured. - 15 VDC is forced on pin 13 and the current flow, $I_{\rm ee}$, is measured. For device types with an external reference - 10 VDC is applied to the external reference input and the current flow, $I_{\rm REF}$, is measured. The limits for power supply currents were enlarged to encompass all manufacturer's devices. Due to differences in implementation of the A/D converter, the loads on the positive and negative supplies will vary from one manufacturer's device to another. The limitations on power supply currents will largely be imposed by the maximum power dissipation specified.

Power Dissipation

Power dissipation can be calculated from the supply currents according to the following equation:

$$P_{D} = (15 I_{CC}) + (5 I_{LOG}) - (15 I_{EE}) - (10 I_{REF})$$
(for devices with external references only)

Input Logic Voltage Levels

In order to test the limits on the input logic levels at which the device will still perform conversions, one conversion is attempted with "clock" and "start convert" inputs at logic "1" = \pm 2.0 V and logic "0"0 = \pm 0.8 V. Accuracy of the final conversion must be insured.

Output Logic Voltage Levels

The output logic levels are checked with all bits on and with all bits off. A 320 uA load is placed at the output with all bits on and the voltage, V_{OH} , is measured. Then a 3.2 mA load is placed on the output with all bits off and the voltage, V_{OL} , is measured.

Output Short Circuit Current

The "A" register is set to 1111 1111 1110 and short circuit output current, is measured for (1) address bits, (2) "End of Convert", and (3) "Serial Data Out".

Input Low Current

Force 0 volts on the "clock" and "start convert" inputs and the current flow, I_{TL} , is measured for each respectively.

Input High Current

Force + 5 volts on the "clock" and "start convert" inputs and the current flow, I_{TH} is measured for each respectively.

Clock Input Pulse Width

All static tests on the ADC will be performed with the minimum input clock pulse width, 200 ns.

Conversion Time

Conversion time is the minimum time required to perform a complete 12 bit successive approximation conversion. A + 2.2 uf solid tantalum capacitor should be connected between DUT pins 15 (+) and 10 (-) for conversion times less than 24 usec. All static tests will be performed at the maximum rated conversion speed.

Power Supply Sensitivity Tests

Power supply sensitivity tests will be performed both with all bits on and all bits off. $V_{\rm CC}$ is varied \pm .45 V and the variation in the ADC transition voltage is recorded, PSS1. $V_{\rm ee}$ is varied \pm .45 V and the variation in the ADC transition voltage is recorded, PSS2. $V_{\rm LOG}$ is varied \pm 0.5 V and the variation in the ADC transition voltage is recorded, PSS3.

Absolute Accuracy

For unipolar devices accuracy will be measured with all bits on only. For bipolar devices accuracy will be measured with all bits on and again with all bits off. The "A" register is set to 1111 1111 1110 and the last transition voltage is measured. Then the "A" register is set to 0000 0000 0000 and the first transition voltage is measured. The accuracy of these measured transition voltages are compared with the specification limits on accuracy.

Zero Error

For a unipolar device zero error cannot be measured directly, extrapolation is required. First and last transition voltages are measured. A straight line is drawn between these points and extended to the voltage corresponding to the ADC address of 0000 0000 0000. Calculated voltage there + 1/2 LSB is the zero error, where an LSB = (Last transition voltage - First transition voltage)/4094. Zero Error = $C_{T1} + LSB/2 - 0$ where C_{T1} is negative for device types 1, 2, 9 and 10.

Device types 7, 8, 15, and 16 are complementary to device types 1, 2, 9 and 10 so logic inputs to reference DAC (address) are complemented and 1/2 LSB is subtracted from the first transition voltage.

$$c_{T1} - \frac{LSB}{2} - 0 = zero error$$

where Or1 is positive

Linearity Testing

The circuit used to measure linearity of the MN5200 series of Analog to Digital converters is shown in Figures 5.4 & 5.5. The S3260 places an address in the "A" register, the input to the reference DAC. The output of the ADC then cycles between the address in the "A" register and that address plus 1 LSB. For example, if S3260 placed 0111 1111 1111 on the input to the reference DAC, the outputs from the ADC will alternate between 0111 1111 1111 and 1000 0000 0000. An abbreviated way of representing this transition is to place an asterisk after the address, i.e. 1000 0000 0000*. The output from the reference DAC is then summed with the input to the ADC in the error amplifier. The resulting error voltage is the amplified sum of the output of the DAC at one particular address and the ADC's transition voltage to the next address. Since the output of the DAC can be calculated at any address, the next ADC transition voltage can be determined by first dividing the error amplifier reading by the amplifier's gain, and then adding the output voltage of the DAC. Linearity for the 5200 ADC is specified as best fit straight line. Linearity will be measured as end point straight line. Best fit linearity will be obtained by adding max positive and max negative deviation from the straight line, dividing the result by two and offsetting the linearity curve accordingly. To measure the end point linearity of the ADC, the first and last transition voltages are used to establish an ideal straight line. All other transition voltages are compared to the ideal straight line.

Two basic techniques for measuring linearity error are employed. The first, called the abbreviated test method, tests only the 42 addresses listed in Table 5.2. These addresses consist of all of the major carries in addition to the two addresses below the major carries and one address above the major carries (where possible). The second, tests all transitions between 0 and full scale. In both cases the calculated ADC transition voltages are compared to the ideal straight line determined by the first and last ADC transition voltages to calculate the linearity of the device.

The initial measurements and adjustments for the "abbreviated test" and the "test all codes" method are identical. At the start of the test the "A" address is set to 0000 0000 0000 and the buffered reference DAC output is set to - 10.0000 V by adjusting the DAC offset potentiometer. This establishes V_{RDAC} (0). A Fluke model 8500A 5 1/2 digit DVM is used to take the measurements with an IEEE bus to interface it to the S3260. The "A" address is then set to 1111 1111 1111 and the buffered reference DAC output is set to + 9.9951V by adjusting the gain potentiometer. This establishes V_{RDAC} (FS). The general expression for the buffered reference DAC output is:

TABLES 5.2. Abbreviated Test - A Address Input Codes

$$V_{RDAC}$$
 (N) = V_{RDAC} (0) + $\frac{V_{RDAC}$ (FS) - V_{RDAC} (0) N [5.3]

$$V_{RDAC}$$
 (N-1) = V_{RDAC} (0) + $\frac{V_{RDAC}$ (FS) - V_{RDAC} (0) (N-1) [5.4]

The voltage V_{RDAC} (N-1) is derived because the ADC cycles between $A \ge B$ and A < B, where B is the ADC output address.

Next, with all relays deenergized, both inputs to the error amplifier are grounded and the output offset voltage, $E_{\rm O}$ (0), is set as close to 0 as possible by adjusting the op-amp offset potentiometer, R 10 . $E_{\rm O}$ (0) is then recorded. This completes the initialization portion of of the "abbreviated test" and the "test all codes".

Abbreviated Test Method

In the abbreviated test the 42 addresses listed in Table 5.2 are generated by the S3260 and sequentially applied to the inputs of the reference DAC. The voltage at the output of the error amplifier, $E_{\rm O}$ (N), is recorded. Now that $V_{\rm RDAC}$ (N-1) and $E_{\rm O}$ (0) are known, the ADC transition voltages can be calculated from $E_{\rm O}$ (N).

$$E_o$$
 (N) - E_o (O) = - $(\frac{R_F}{R_I})$ (V_{RDAC} (N-1) + V_{ADCIN} (N)) [5.5]

or
$$V_{ADCIN}$$
 (N) = - $(\frac{R_{I}}{R_{F}})$ (E₀ (N) - E₀ (0)) - V_{RDAC} (N-1) [5.6]

Transition voltages on the ideal linearity curve will hereafter be referred to as C_T (N). C_T (1) = V_{ADCIN} (1) and C_T (4095) = V_{ADCIN} (4095) since the first and last transition voltages establish the ideal end point linearity curve. The other transition voltages on the ideal linearity curve can be calculated from the expression:

$$c_{\rm T}$$
 (N) = $\frac{c_{\rm T}}{4095} - c_{\rm T}$ (1) (N-1) + $c_{\rm T}$ (1)

Bit errors (deviations from the ideal straight line) can now be determined:

$$\epsilon_{(N)} = \frac{V_{ADCIN}(N) - C_{T}(N)}{ISB} \quad \text{in LSB's} \quad 5-8$$

where LSB =
$$\frac{v_{ADCIN} (4095) - v_{ADCIN} (1)}{4094}$$

After all bit errors have been calculated, the addresses of the maximum positive bit weight error and the maximum negative bit weight error can be determined.

To generate the word for maximum positive bit weight errors a logic "1" is placed in the address if the corresponding bit weight error is positive. All other address bits are set to logic "0".

To generate the word for maximum negative bit weight errors a logic "1" is placed in the address if the corresponding bit weight error is positive. All other address bits are set to logic "0".

The latter two addresses (-1 LSB) are applied to the "A" address register in turn and the error voltages are measured. ADC transition voltages and bit errors are calculated as before.

The offset voltage, BFOE, to achieve "Best Fit Linearity" will be obtained as follows:

BFOE =
$$\frac{\mathbb{Z} + NL + \mathbb{Z} - NL}{2}$$
 in mV

Allow 1 sec before each measurement (or more if necessary).

Major Carry Errors (MCEN) are the differences in size between an LSB at a major carry and an LSB averaged over the entire range of the ADC. They are calculated from the ADC transition voltages according to the following equation:

MCE (N) =
$$\frac{V_{ADCIN} (N + 1) - V_{ADCIN} (N) - LSB}{LSB}$$

The LSB carry, MCE (12), cannot be calculated

The previous measurements and calculations of bit weight errors and major carry errors are affected by hysteresis. The following calculations derive static bit weight errors and static major carry errors. The major carry transition is ignored and the transition after the major carry is measured. The difference between the two transitions before the major carry provides the valve used for an LSB. The static bit weight errors are calculated as follows:

$$(N)_{STATIC} = \frac{V_{ADCIN} (N)_{STATIC} - C_{T} (N)}{LSB_{STATIC}}$$

where LSB_{STATIC} = V_{ADCIN} (N-1) - V_{ADCIN} (N-2)

and
$$V_{ADCIN}$$
 (N)_{STATIC} = V_{ADCIN} (N + 1) - LSB_{STATIC}

From the equation for LSB_{STATIC} it can be seen that static bit weight errors cannot be determined for the 2 last significant bits of an address.

Static major carry errors can be calculated in a similar fashion:

where LSB_{STATIC} is calculated as it was for static bit weight errors.

Measure All Transitions

After the ADC is allowed to warm up for a sufficient amount of time, the S3260 sequentially applies all addresses to the "A" register. The error voltage is measured and recorded at each address, and from these error voltages the ADC transition voltages can be determined as before. Bit Errors (static and dynamic), maximum positive and negative bit weight errors, nonlinearity, and major carry errors (static and dynamic) are all determined as they were in the abbreviated test method.

SECTION VI

12 Bit D/A Converter

Table of Contents

		Page
6.1	Background and Introduction	VI-1
6.2	Description of Device Type	VI-3
6.3	Characterization of the 562	VI-4
6.3.1	Static Test Parameters	VI-4
6.3.2	Dynamic Test Parameters	VI-7
6.3.3	Static Test Circuit	VI-7
6.3.4	Settling Time Test Circuit	VI-8
6.3.5	Devices Used for Testing	VI-9
6.4	Automatic Test Development	VI-9
6.4.1	Test Program Development	VI-14
6.4.2	Monotonicity	VI-24
6.5	Evaluation of Data	VI-2
6.5.1	Dynamic Test Data	VI-27
6.5.2	Static Test Data	VI-27
6.6	Conclusions and Recommendations	VI-31

List of Figures

Figure	Title	Page
6.1	Simplified Interconnect Schematic	VI-11
6.2	Test Circuit For Static Tests	VI-12
6.3	Waveforms For Settling Time, Device Types 01 and 02	VI-35
6.4	Test Circuit For Settling Time, Device Types 01 and 02	VI-36
6.5	S3260 Test Adapter For The 562, D/A Converter	VI - 37
6.6	Reference Module Converted To The S3260 Test Adapter	VI -3 7
6.7	Photographs of Typical Settling Time Waveforms (Device Type 01)	VI - 38
6.8	Bit Weight Error Display (+ 25°C)	VI - 52
6.9	Bit Weight Error Display (+ 125°C)	VI - 53
6.10	Bit Weight Error Display (- 55°C)	VI - 54
6.11	Major Carry Error Display (+ 25°C)	VI - 55
6.12	Major Carry Error Display (+ 125°C)	VI-56
6.13	Major Carry Error Display (- 55°C)	VI-57
6.14	Linearity Distribution For 12 Devices Tested (+ 25°C)	VI-58
6.15	Linearity Distribution For 12 Devices Tested (+ 125°C)	VI - 59
6.16	Linearity Distribution For 12 Devices Tested (- 55°C)	VI-60

List of Tables

Table	Title	Page
	Test Conditions, Equations, and Limits	VI-33
6.1	Output Settling Time Data	VI - 39
6.2	·	VI-40
6.3	Device Type Ol Data at + 25°C	VI-44
6.4	Device Type Ol Data at + 125°C	VI - 48
6.5	Device Type Ol Data at - 55°C	VI 40

SECTION VI

CHARACTERIZATION OF 12-BIT D/A CONVERTERS

MIL-M-38510/121

6.1 Background and Introduction

The increased use of microprocessors in military systems has stimulated interest in JAN 38510 specification development of data converters and associated devices which are needed to interface analog sources, sensors, loads, and displays with digital processing hardware. In 1978, the first JAN D/A Converter slash sheet was developed, MIL-M-38510/113. The DACO8 and DACO8A devices, 8-bit monolithics with dual complementary current outputs, fully voltage compliant, low cost and multi-sourced were selected for the slash sheet.

The need for higher-resolution D/A Converters will be filled by MIL-M-38510/121, 12-bit D/A Converters. Monolithic 12-bit converters have only recently begun to displace the hybrid devices which have predominated the marketplace in past years, and there is reason to believe this trend will continue. The 562 is one of the first 12-bit monolithics that is multi-sourced and has been identified by users as a desirable component for military systems.

While multi-sourcing has many advantages, it presents some difficulty in preparing a common specification, at least for linear devices and in particular for data converters. Of three manufacturers which offer the 562, no reasonable compromise of specifications could be negotiated to include even two manufacturers on one device type. Consequently, there are two device types in the slash sheet, each sourced by only one manufacturer; the third device is not included at this time for reasons explained within the following text.

The development of test circuits and techniques for 12-bit data converters has been a considerably more difficult task than that for 8-bit devices. For example, when one is measuring linearity to limits of 1/2 LSB, it is desirable to have a test method accurate to *0.05 LSB, or approximately *0.001%. Noise and differences in ground voltages alone can degrade the measurements, not to mention drift and meter accuracy/linearity. These concepts are also addressed within the text.

An attempt was made in this device characterization to measure linearity both with the "Abbreviated Linearity Test Method", using bit weight errors and superposition, and with the "All Codes Linearity Test Method" to see if the data correlated well. How well the data correlates will

be largely determined by how much superposition error is present. Superposition errors referred to here are bit interactive errors. The devices tested correlated well but it is to be expected that some manufacturers devices will not correlate well. Devices with appreciable interactive errors may not pass the Abbreviated Linearity Test because of the \leq (+) NL + \leq (-) NL test. Restricting the summation of Bit Weight Errors to \pm 0.1 LSB will be difficult to pass if interactive errors are appreciable. However, failing to meet this requirement does not necessarily mean that the device will not meet the overall linearity requirement of \pm 0.5 LSB. It is for that reason that the device then be subjected to an All Codes Linearity Test. A failure therein would be final.

In like manner implementation of a \pm 0.9 LSB differential non-linearity (MCE) insures that a device with a marginal error will not be judged monotonic (or non-monotonic) when non-linearities and measurement errors may make the device look better (or worse) than it really is. If the MCE is within the range \pm 0.9 to \pm 1.1 LSB the device then would be subjected to an all codes linearity and monotonicity test. The all codes monotonicity test as implemented herein is much more accurate. A failure therein would be final.

6.2 Description of Device

The 562 is a monolithic 12 bit D/A Converter with guaranteed monotonicity over the full military operating temperature range, -55 to 125°C. The device is mounted in a hermetically sealed ceramic 24 lead dual inline package. The 362 accepts a reference voltage of 0 to + 10 V and provides a binary weighted output current proportional to the product of the digital address input and the reference voltage. When the reference voltage is variable the device is a two quadrant DAC. On the other hand, when the reference voltage is fixed the device is simply a DAC with a nominal output current of -2 mA. Laser-trimmed internal gain, voltage-range and bipolar offset resistors are incorporated to provide accurate output voltages when used in conjunction with an external amplifier. Scaling errors are minimized because of low resistor tracking TCR; approximately 1 ppm/C°. The following ranges can be pin-programmed;

0 to + 10 V, 0 to + 5 V,
$$-5$$
 to + 5 V, -2.5 to + 2.5 V, -10 to + 10 V

The digital code for the device is natural binary "positive true". In the bipolar mode the digital code is offset binary

Address In	Unipolar	<u>Bipolar</u>	
0000 0000 0000	o v	- 10.000 V	
1000 0000 0000	+ 5.000 V	0 V	
1111 1111 1111	+ 9.99878 V	+ 9.99572 V	

The device is CMOS or TTL compatible. With pin 2 connected to pin 1 the device is CMOS compatible and the internal logic threshold is $\frac{V_{CC}}{2}$ and the voltage may be 4.75 to + 15.8 V. With pin 2 open for device type 01 and grounded for device type 02 the logic threshold is approximately + 1.4 V and the device is TTL compatible with V_{CC} = + 5 V \pm 10%. The 562 is available in both binary and BCD versions.

The 562 current output is the weighted sum of the outputs of three similar groups of binary scaled quad current generators, controlled by V_R . The logic inputs steer these currents through non-saturating bipolar-transistor current switches to either ground or the respective quad output bus. The output currents from the 2nd and 3rd quads are attenuated by 16:1 and 256:1 respectively for binary and by 10:1 and 100:1 respectively for BCD. The attenuated outputs are then summed with the unattenuated output of the 1st quad. The output current is then the sum of 12 individually switched currents having a binary relationship.

The current generating transistors from each quad group have emitter areas in the ratio of 8:4:2:1. The ladder network resistances are in the ratio of 1:2:4:8. With equal voltages applied to the resistors, the emitter currents are therefore in a binary ratio. Because of the weighted emitter area, the transistors operate at equal emitter current densities and therefore have nearly equal $V_{\rm BE's}$ and $h_{\rm FE's}$. The control amplifier (A1) drives the bases of the constant current transistors and a reference transistor, which has $h_{\rm FE}$ and $V_{\rm BE}$ matched to those of the constant current and bit switching transistors.

 ${
m V_R}$ is applied to the externally trimmable gain resistor (Rl) to set a reference current of 0.5 mA. Amplifier Al establishes the appropriate base voltage to force collector current of Ql equal to IR. Variations in hFE, ${
m V}_{\rm AE}$, or supply voltage with time and/or temperature are sensed in the reference amplifier circuit and the reference amplifier adjusts ${
m V}_{\rm BE}$ to maintain the collector current of Ql (and therefore the bit currents) constant in the presence of these variations.

6.3 Characterization of the 562

6.3.1 STATIC TEST PARAMETERS (See Table 6.1)

Supply Current (Icc)

The current drain on the $V_{\rm CC}$ supply is measured with all bits on in the CMOS made since it represents the worst case. $V_{\rm CC}$ = + 15 V.

Supply Current (IEE)

The current drain on the $V_{\rm EE}$ supply is measured with all bits on in the CMOS mode. $V_{\rm EE}$ = - 15 V.

Logic "1" Input Current (IIH)

Logic "1" input current is measured in the CMOS mode with V_{cc} = + 15 V since it represents a worst case.

Logic "0" Input Current (ITL)

Logic "0" input current is measured in the CMOS mode with $\rm V_{cc}$ = + 15 V. Since it represents a worst case.

Full Scale Current (IRS)

DUT output current is measured with all bits on. Subtracting the value of output current with all bits off from that obtained with all bits on provides a measure of $I_{\rm FS}$.

Unipolar Zero Current (Ioz)

Unipolar zero current is leakage current in the unipolar mode with all bits off. It is specified as a percent of measured full scale current (IFS) at + 25°C and is specified separately for CMOS and TTL modes.

Unipolar Zero Current Drift $A_{I_{FS} \triangle T}$

Unipolar zero current drift is the average temperature coefficient of unipolar zero current. The average temperature coefficient is measured from + 25 to + 125°C and from -55 to + 25°C. Neither value shall exceed the limits specified in Table II. IFS in the expression for unipolar zero current. drift is $\rm I_{FS}$ at + 25°C.

Gain Error (Ge)

The 562 D/A converter provides a current output that is proportional to the digital address applied to it. The output current has a \pm 25% tolerance but provided within the device is a tapped span resistor which may be use; in conjunction with an external operational amplifier. The span resistor is laser trimmed to offset the loose tolerance on output current and provide a voltage gain tolerance of \pm .25% at the amplifier output. Unipolar gain is measured and it is defined as the difference between the output voltage with all bits on and the output voltage with all bits off with an applied reference voltage of + 10.000 VDC. Gain error is specified in ppm of Full Seale Voltage (FSV), + 10V. Gain error is specified separately for CMOS and TTL modes.

Gain Error Drift (△G€ FSV △ T

Gain Error Drift is the average change in gain as a function of temperature. The average temperature coefficient is measured from +25 to $+125^{\circ}$ C and from -55 to $+125^{\circ}$ C. Neither value shall exceed the limits specified.

Bipolar Offset Error (BPOE)

Bipolar Offset Error is the voltage measured at the DUT output (pin 9) with + 10.000 V applied to the bipolar offset resistor (pin 7) and - 10.000 V applied to the 20 volt span resistor (pin 11) with DUT pins 8 and 9 connected together. BPOE includes the effects of unipolar zero (leakage) current.

Bipolar Offset Drift $\left(\frac{\Delta BPO}{FSVR \Delta T}\right)$

Bipolar Offset Drift is defined as the change in offset voltage with respect to full scale per centigrade degree temperature change.

Power Supply Sensitivity From V_{CC} In TTL Mode (+PSS1)

The change in output voltage is measured for a \pm 10% change in V_{CC} from nominal + 5 VDC with V_{EE} at nominal - 15 VDC. Measurement is made with all bits off and also with all bits on. Neither change in output voltage shall exceed the limits specified in Table 6.1.

Power Supply Sensitivity From V_{CC} in CMOS Mode (+PSS2)

Same as PSS1 except $V_{\rm CC}$ nominal is + 15 VDC and DUT pins 1 and 2 jumpered together.

Power Supply Sensitivity From VEE in TTL Mode (-PSS1)

The change in output voltage is measured for a \pm 10% change in V_{EE} from nominal - 15 VDC with V_{CC} at + 5 VDC. Measurement is made with all bits off and also with all bits on. Neither change in output voltage shall exceed the limits specified in Table 6.1.

Power Supply Sensitivity From VEE IN CMOS Mode (-PSS2)

Same as -PSS1 except that $V_{\rm CC}$ is set at a nominal value of + 15 VDC and DUT pins 1 and 2 are connected together.

Summation of Positive Bit Errors (Z NL+)

Assuming negligible superposition errors, the application of the address with logic "1"s for those bits which when tested alone exhibited positive bit errors should yield the maximum positive deviation from the ideal linearity curve, a straight line between zero and full scale.

Summation of Negative Bit Errors (ENL-)

Assuming negligible superposition errors the application of the address with logic "1"s for those bits which when tested alone exhibited negative bit errors should yield the maximum negative deviation from the ideal linearity curve, a straight line between zero and full scale.

Bit Interaction (NL(+) + NL(-))

At full scale **Z** NL(+) + **Z** NL(-) is assumed to be zero. It follows that this relationship shall hold over the full range of the DUT. Any deviation from this relationship, aside from measurement error, shall be assumed to be due to non-linearity (superposition errors). Devices which exhibit a bow in the linearity curve from zero to full scale will exhibit superposition errors. Assuming a measurement accuracy of ± .05 LSB, the limits applied to this parameter were chosen to be large enough to measure the existence of superposition errors. Failure to pass this test does not constitute a module failure but requires the additional all codes linearity and monotonicity testing. A failure to pass

the latter constitutes a module failure. Successful completion of the all codes tests insures that the device is linear to within specified limits and is monotonic.

Major Carry Errors (MCE)

The major carry test is intended to insure that the DUT is monotonic. To be monotonic the output voltage increment must be greater than 0 V for each increment of DUT address from all "0"s to all "1"s (0 to 4095). Assuming negligible superposition errors and no dynamic errors, the incremental voltages at the major carries, MCl-MCll, should represent the worst case differential nonlinearity. A differential non-linearity of less than \pm 1 LSB insures monotonicity. Since non-monotonicity can be disastrous in many device applications and the measurement accuracy of the tester is \pm .05 LSB (max), a tolerance of \pm 0.9LSB is placed on this parameter. Failure to pass this test within \pm 0.1 LSB will not constitute a failure but will require the vendor to test all codes monotonicity and linearity. Successful completion of the latter insures that the device is monotonic.

6.3.2 DYNAMIC TEST PARAMETERS (+ 25°C only)

The settling time test measures the response time between the 50% point of the input transition (all bits on to all bits off or all bits off to all bits on) and the point in time at which the output settles to within \pm 1/2 LSB of final value. For a device type 01, \pm 0.24 uA = \pm 1/2 LSB corresponds to \pm 1.22 mV. For a device type 02, \pm 0.61 uA = \pm 1/2 LSB and with a 2K load \pm 1/2 LSB corresponds to \pm 1.22 mV.

6.3.3 STATIC TEST CIRCUIT

The static test circuit shown in Fig. 6.2 is a simplified version of the test circuit utilized on the S3260. Not shown are the ground drivers that were required because of the physical separation of the reference DAC, the test adapter circuitry and the DUT. Also not shown is a voltage follower buffer inserted between the reference DAC reference voltage output (pins 52, 53 on DAC 1138) to minimize output voltage shifts due to loading. Table 6.2 indicates the relay states for the various parameters to be tested.

Al is the error amplifier which converts the DUT output current to voltage and compares it to the corresponding Ref. DAC output and amplifies the difference. The amplified difference voltage is used to provide an accurate measure of DUT gain, linearity, power supply sensitivity, and in a slightly different circuit configuration to test BPOE. With all relays deenergized the error amplifier inputs are both connected to ground the through $3\kappa\Omega$ resistors and the amplifier offset voltage may be trimmed to zero. The offset trim is a 20 $\kappa\Omega$ potentiometer connected between amplifier pins 1 and 8 with the wiper tied to + 15 V.

A2 is a unity gain inverting amplifier that is employed only for BPOE measurements. It provides an accurate -10.000 VDC.

A3 and A4 are Reference Voltage and Reference DAC output buffer amplifiers. They are tested and trimmed (if necessary) at the start of any sequence of device testing, utilizing a Fluke 8500 DVM (or equiv.). Once done the test/cal need not be repeated for subsequent DUT tests.

Input and output currents were measured by forcing the appropriate voltage levels and measuring currents. Just how these tests are implemented will be governed by the equipment available to the tester.

6.3.4 SETTLING TIME TEST CIRCUIT

Figure 6.3 shows the settling time test circuit employed by GEOS to test device types 01. D1 biases Q1 such that the emitter of Q1 (DUT output) is maintained approximately at OV. Q1 is a common base amplifier which converts DAC output current variations to voltage variations. The common base amplifier was selected because of its excellent high frequency response. The collector voltage swing is clamped to within a Schottky voltage drop of + 5 VDC. Capacitance in the collector circuit of the Q1 transistor should be minimized because of the large value of R. For a device type 01 R = 5K and for a device type 02 R = 2K. V_L A+ 15 V for "turn on" (all bits off to all bits on) and + 5 V for "turn off" (all bits on to all bits off). Q2 and Q3 provide differential buffering of the Q1 output.

To test all bits off to all bits on settling time V_L is adjusted for a Q1 output voltage of $+5\,\mathrm{V}$ with all bits on $(V_C\,\Sigma\,+15\,\mathrm{V})$ and $R_L=5\mathrm{K}$. A square wave voltage is applied to the DUT address inputs (V_{ins}) and the scope preamp is adjusted so the flat portion of the waveform corresponding to all bits on is on the center line of the screen with a sensitivity of 1 mV/cm. The positive edge of V_{in} is used to trigger the scope and the sweep start is marked on a vertical graticule of the scope trace. Settling time is then measured, the time required for the output to settle to within \pm 0.5 LSB (or \pm 1.22 mV).

To test "all bits on to all bits off" settling time V_L is adjusted for a Q1 output voltage of +5V with all bits off and $R_L = 5K$. A square wave voltage is then applied to the address inputs (V_{in}) . The scope trace is adjusted to locate the flat portion of the output waveform corresponding to "all bits off" on the center line with a vertical sensitivity of 1 mV/cm. The sweep trigger alignment may need readjustment since the scope must trigger on the negative edge of V_{in} . Settling time is then measured, the time required for the output voltage to settle to within \pm 1/2 LSB (\pm 1.22 mV). Figure 6.3 shows the waveforms and Figure 6.7 shows photographs of typical settling times measured.

6.3.5 DEVICES USED FOR TESTING

There were 13 devices tested of which 6 were obtained directly from Analog Devices, 6 were obtained from Analog Devices through RADC, and 1 was purchased by GEOS. Data is only tabulated for 12 devices because one of the six devices obtained directly from Analog Devices with + 25°C data failed during the course of test program development. Repeated rapid cycling between + 25°C, + 125°C and - 55°C may have been responsible for the failure: Device S/N 4311 failed.

S/Ns 4310 - 4315

Samples obtained from Analog Devices

with + 25°C data

S/Ns 19, 20, 21, 25, 36 & 48

Samples obtained from RADC

s/n 5

Purchased sample

All devices characterized were Analog Devices only.

The devices with S/Ns 4310 - 4315 appeared to be significantly better than the others in settling otherwise differences were not significant.

Three device type 02s were tested and found to be out of specification. However, the origin of the devices is unknown. Harris has been asked to submit samples with data (if possible) for characterization.

6.4 Automatic Test Development

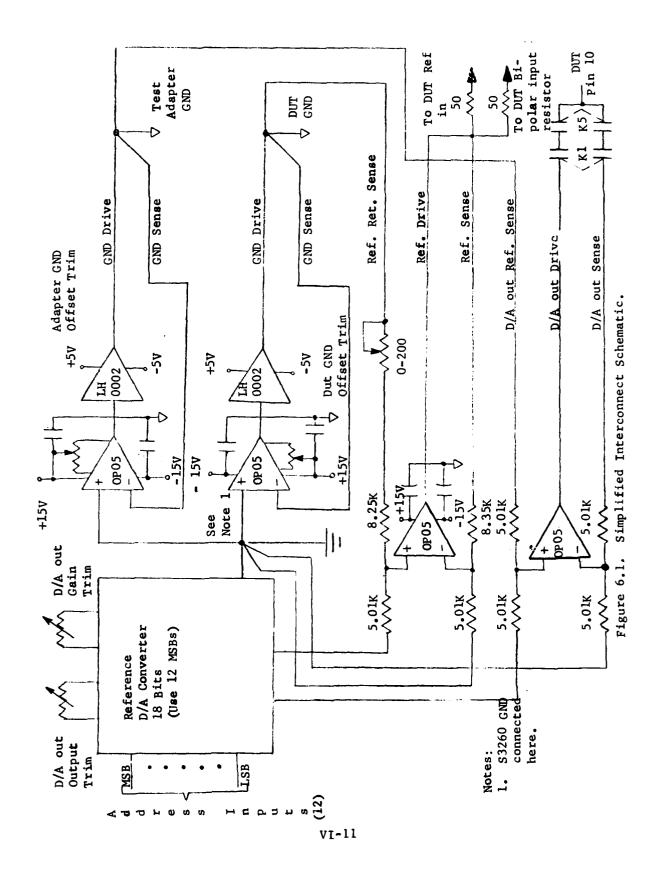
One of the primary considerations in attempting to test a 12 bit D/A Converter on the Tektronix S3260 is, "How does one measure DAC output linearity to ± .001% and fast enough" that the S3260 isn't tied up for long periods of time. GEOS chose to implement a comparative type test which utilizes a Reference Module in conjunction with the S3260 test adapter to test the device's linearity and accuracy. The reference module contains an 18 bit D/A Converter (12 MSBs used) some switches, some buffer amplifiers, and active ground drivers. It was designed to interface with D/A and A/D Converters with 12 bits or more. It contains switching, logic, and buffer amplifiers and is capable of interfacing accurately with A/D and D/A converters of various ranges and codes. It was primarily designed to interface with the 562 series of 12 bit D/A Converters and the 5200 series of 12 bit A/D Converters. See Figure 6.6.

Another consideration in testing devices with such accuracy on the S3260, or any other automatic tester for that matter, is grounding and line drops. If the test circuits were designed for bench test. the circuitry would be kept close together and unipoint grounding employed. All of the precautions would be taken to minimize voltage drops on critical wires, avoid ground loops, and prevent oscillations. However, maintaining the close proximity and unipoint grounding on the S3260 is next to impossible. Therefore an alternate approach was taken. Active ground drivers (See Fig. 6.1) consisting of a cascaded connection of an OP 05 amplifier and a hybrid driver (LH0002) in the voltage follower configuration were employed to drive the DUT and adapter grounds separately to the same ground potential as the reference module ground. Care was taken in the selection of adapter devices to minimize power consumption (by using low power Schottky for example) and keeping the driven grounds disconnected from machine ground. Offset voltage trims were implemented on the OP 05s to enable adjustment of the JT and adapter grounds to 0 V relative to the Ref. D/A ground. The technique worked exceptionally well and contributed largely to the ultimate success in obtaining better than ± .05 LSB measurement accuracy on linearity measurements. A 12 bit D/A converter in the unipolar mode on the 0 to 10 V range has an LSB voltage increment value of 2.44 mV. \pm .05 LSB equals \pm 122 mV, a very small voltage.

Also employed, as shown in Figure 6.1 are buffer amplifiers for the Reference D/A output and the Reference Voltage output. The amplifiers are differential and remote ground and output sense lines are employed to prevent line drop from deteriorating measurement accuracies.

It should be noted that the reference module when used with the S3260 test adapter provides a simple setup for bench testing. Aside from some test equipment, all that is required is the undersocket card interface. This feature enables the DUT to be tested with access to all of the adapter circuitry on the under socket card that is not readily accessible on the S3260.

The method employed for testing the linearity and accuracy of the 562 is illustrated in Figure 6.2. The Reference D/A output voltage is fed to the 10 volt span resistor (DUT pin 10) via relays K1 and K5. Both Reference D/A output drive and Reference D/A output sense lines are switched separately and connected together at DUT pin 10. For any given DUT address the difference between the DUT output and the Reference D/A output are compared, inverted and amplified. Use of the 10 volt span resistor is possible because the span resistors are laser trimmed to compensate for full scale current deviations from nominal and provide nominal output voltage when used in conjunction with a zero offset external op amp. If full scale current is low by 10% from nominal then the span resistor will be high by 10%. With



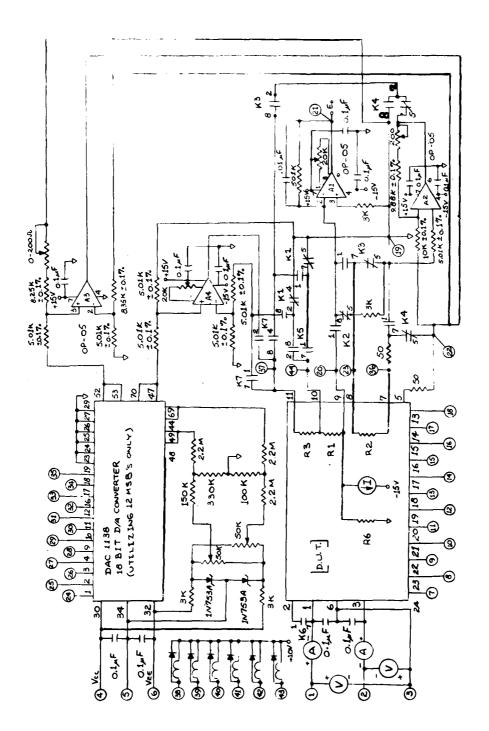


Figure 6.2. Test Circuit For Static Tests.

all relays deenergized the error amplifier offset voltage is trimmed to 0V, $E_0 = 0$ V. The Reference voltage is adjusted to + 10.0000 V a adapter pin 22, as read on a Fluke 8500ADVM. The Reference D/A address inputs are set to all zeros, relays Kl and K5 are energized and the Reference D/A output voltage at DUT pin 10 is adjusted to (offset adj) to - 10,000 V, as read on the Fluke 8500. The Reference D/A address inputs are then set to all ones and the Reference D/A output voltage at DUT pin 10 is adjusted (gain adj) to + 9.9951 V, as read on the Fluke 8500. The Reference D/A output voltage, the Reference voltage, and the error amplifier have been calibrated and the test proceeds. With the DUT address bits all zeros, the Reference D/A output voltage is incremented by a small but finite voltage and the change in voltage at the error amplifier output noted. Dividing the change in output voltage by the change in input voltage provides the error amplifier gain (inverted) which is necessary to accurately measure the Reference D/A output voltage divided by the 10 V span resistance for a given address is compared to the DUT output current for a corresponding address. It should be noted here that the Reference DAC employed required complimentary logic. In Table codes are shown as such, eg all 0's applied to the DUT provides a nominal - 9.997 KV (equivalent) output. All 1's applied to the Reference D/A provides a nominal + 9.9975 V output and all "O"s applied to the Reference D/A provides a nominal 0 V.output. The reference module enables a complimentary of the Reference D/A address inputs to enable the same address codes to be applied to both.

To measure linearity, the DUT equivalent output voltages (I_{O} R_{1}) at zero and full scale are obtained by measuring E_{O} (adapter pin 31) for all DUT and Reference D/A out bits off and for all DUT and Reference D/A out bits on respectively. The DUT equivalent output voltages are calculated using the following relationship

$$I_0 R_1 = - (\frac{E}{G} + \text{Reference D/A out})$$

A straight line is established between these two points and subsequent measurements of DUT outputs for any given address can be compared to the straight line which is the ideal linearity curve. The equations for linearity and gain accuracy are given in more detail written the automatic test program development portion of this report.

One other important factor to consider in testing 12 bit D/A converters is temperature stability. Warm up time before test varies from vendor to vendor. The device dissipates as much as 600 mW and it will take a finite amount of time for temperature to stabilize upon turn on. Just how long the stabilization period allowed should be depends upon how fast the codes are tested. Vendors using the abbreviated test method for measuring linearity are not as sensitive but not insensative to thermal shifts. In testing the devices on the S3260

in the all codes linearity test mode the data obtained was very sensitive to stabilization time just as the data would be in a bench test setup. All final test data was taken, abbreviated and all codes, after a soak at temperature of 12 minutes. The long stabilization period was probably due to the fact that the temptronics unit cools the DUT directly but does not cool the lower portion of the DUT connector: There is a steady flow of room underneath. The stabilization time is probably related to the time it takes for some equilibrium condition to occur.

6.4.1 Test Program Development

A test program was developed for the Tektronix S-3263 to enable automatic testing of the 562, 12 bit monolithic D/A converter. Figure 6.2 shows the schematic diagram of the test circuit which includes the Reference Module and the S-3263 Test Adapter (see Figure 6.5 and 6.6 for photographs).

A calibration sequence is always run at the start of testing to insure that the zero and full scale output voltages of the Reference DAC and the DUT reference voltage are accurate. Adjustments are provided on the Reference Module for trimming the latter voltages. For calibration there are jacks provided on the Test Adapter to connect an external, highly accurate, DVM (e.g. Fluke Model 8500A or HP Model 3455A).

The test program proceeds as follows:

1. Power Supply Current from V_{cc} (I_{cc})

 $\rm I_{CC}$ is measured with all DUT address inputs at logic 1's. +15VDC is forced to pin 1 and $\rm I_{CC}$ is measured. (K5 is energized)

2. Power Supply Current from Vee (IEE)

 I_{EE} is measured with all DUT address inputs at logic 1's. -15 VDC is forced to pin 6 and I_{EE} is measured. (K5 is energized)

3. Logic "1" Input Current, I_{LH} (CMOS)

Logic "1" input current is measured by forcing +15 VDC on I/O pins 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, and 35, one at a time and measuring I_{LH} . (K6 energized)

4. Logic "0" Input Current, I_{LL} (CMOS)

Logic "0" input current is measured by forcing 0 VDC on pins 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, and 35, one at a time, and measuring $I_{1,1}$. (K6 energized)

5. Full Scale Output Current, IoFS (TTL)

Full scale out current is measured by setting the DUT address inputs to all 1's, forcing the output pin 22 to 0 VDC, and measuring the current flow, I_{OFS} . V_{CC} = + 5 V (No relays energized)

6. Zero Scale Output Current, IoZ. (TTL)

Zero scale output current is measured by setting the DUT address inputs to all 0's, forcing the output pin 22 to 0 VDC, and measuring the current flow, $I_{\rm OZ}$. $V_{\rm CC}$ = + 5 V (No relays energized)

7. Zero Scale Current, IoZ (CMOS)

Same as 6, except $V_{cc} = +15 \text{ V}$ and (K6 energized)

8. Zero Scale Drift $(\frac{I_{OZ}}{I_{FS}(25^{\circ}C)\Delta T})$

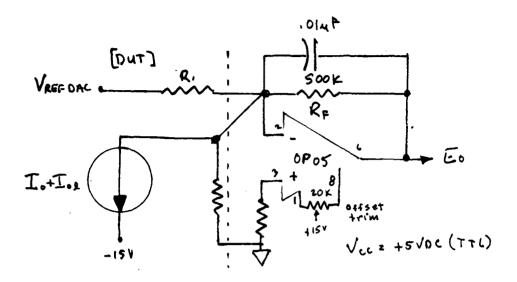
Test is performed as in 6 & 7 and the value of I_{OZ} noted for each temperature at which test is performed. For temperature ranges tested within the operating temperature range of -55 to +125°C the drift shall not exceed the limit specified in Table 1.

9. Bipolar Offset Current, IBIP.

The reference voltage, + 10 V, is applied at pin 19 and appears across the bipolar offset resistor (R₂) and a 50 Ω series resistor with K3 and K 4 deenergized. I $_{\rm BIP}$ = $\frac{\rm V_R}{\rm 0.5K}$ where V_R is the measured voltage drop across the 50 Ω resistor.

10. Gain Error (GE) in TTL mode

Unipolar gain error is measured with the test circuit configured as in Fig. 2 (K1, K2 and K5 energized)



Simplified schematic.

- (a) Set DUT and REF DAC address inputs to all zeros (output off) and measure $E_0(o)$. This voltage included REF DAC offset, OPO5 offset, and DUT Unipolar Offset.
- (b) Set DUT and REF DAC address inputs to all ones (outputs on) and measure $E_{\rm O}({\rm FS})$.

$$E_{O} = E_{O}(FS) - E_{O}(O)$$
 [6-1]
Let $\frac{1}{R_{X}} = \frac{1}{R_{I}} + \frac{1}{R_{O}}$

The equation for output voltage can then be written:

$$E_{O} = G1 \left[V_{REF}(\bar{n}) + V_{ROS} + (I_{O}(n) + I_{OZ}) RI \right] \pm \left[\frac{R_{X} + R_{F}}{R_{X}} \right] V_{XO}$$

$$= -I_{O}(n) R_{F} + G1 V_{REF}(\bar{n}) + \frac{V_{ROS} G1 - I_{OZ} R_{F} \pm (\frac{R_{F} + R_{X}}{R_{X}}) V_{XO}}{FIXED OFFSET} \left[6-2 \right]$$

for any address . Amplified noise, offset current, offset drift, and Zi are neglected.

where

 I_{OZ} = DUT leakage current (all bits off)

V_{ROS} = REF DAC offset voltage

and V_{XO} = external op amplifier input offset voltage (OP-05). Combining offset and leakage terms:

$$E_o(o) = -I_{oZ} R_F - V_{ROS} \left(\frac{R_F}{R_1}\right) \pm \left[\frac{R_F + R_X}{R_X}\right]$$
 [6-3]

Substituting in eg 6-2

$$E_o = I_o R_F - V_{REF} \frac{R_F}{R_1} + E_o(o)$$
 [6-4]

Since the exact value of R_1 is not known, the gain $\frac{R_F}{R_1}$ must be measured. With all bits off on the DUT and the REF DAC measure $E_O(o)$. Leaving the DUT in off state, address REF DAC input with 0000 0000 1110 and measure $E_O(14)$.

$$G1 = \frac{R_F}{R_1} = -\frac{(E_o(14) - E_o(o))}{(\frac{+10}{4096})(2^3 + 2^2 + 2^1)}$$

Assuming that $+\frac{10.00}{4096}$ is an LSB of REF DAC

S3260 measurement accuracy for Gl ≈ ± 0.4%

then

$$E_{o} = E_{o} \text{ (FS)} - E_{o}(o) = -\left[(I_{o}(FS) - I_{o}(o)) R_{F} + V_{REF}(FS) \frac{R_{F}}{R_{1}} \right]$$
FS output voltage = $I_{o}(FS) - I_{o}(o) R_{1} =$

$$(referred to error amp. input) = \frac{E_{o}(FS) - E_{o}(o)}{G1} - V_{REF} (FS)$$

=
$$V_{REF}$$
 (FS) + I_o (FS) R_1

$$G_{\epsilon} = \frac{E_{o}(FS) - E_{o}(o)}{G1}$$

(spec. is given in mV)

Device Types 01 Max error amplifier output voltage.

If $R_F = .5M$ and $R_1 = 5 K \pm 25\%$ (Init. Tol.)

 E_0 (max) = G1 (max) x Unipolar gain error (max)

$$= - \frac{0.5M}{(3.75K)} \pm 25 \times 10^{-3} = \pm 3.333 \text{ V for max. unipolar gain error and max. gain.}$$

Error amplifier is not going to saturate.

Device Types 02

If $R_F = 500K$ and $R_1 = 25K \pm 25\%$ (Init. Tol.)

 E_0 (max) = G1 (max) Unipolar gain error (max)

[6-9]

= - F 8.333 V for max unipolar gain error and max gain.

Error amplifier is not going to saturate.

Machine error contribution to the latter measurements is less than 2% of the unipolar gain error (negligible).

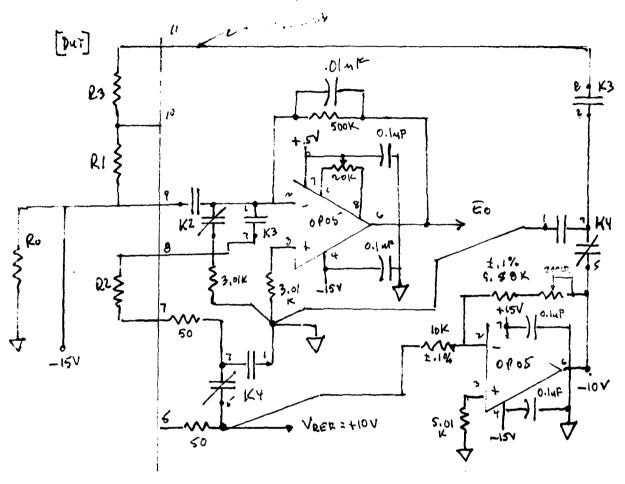
11. Gain Error (G_E) in CMOS mode

This measurement is performed similar to (10), but with $V_{\rm cc}$ = + 15 VDC, $V_{\rm IH}$ = + 10.4 , and K6 energized.

12. Gain Error Drift $(\frac{G_{\in}}{FSVR}\Delta T)$

The unipolar gain error drift is derived by measuring unipolar gain at the -55°C, + 25°C, and +125°C and calculating the average temperature coefficient for each excursion from +25°C separately. Namely, the temperature coefficient from + 25°C to -55°C and the temperature coefficient from + 25°C to + 125°C. The largest of the two measured values is displayed. Step 10 or 11 describes the method used for measuring unipolar gain for TTL or CMOS interfaces respectively.

13. Bipolar Offset Error, BPOE



BPOE test circuit.

BPOE, as specified in Table I is the DUT output offset voltage will all bits off, + 10 V \pm .01% applied through 50 Ω to the bipolar offset resistor (DUT pin 7), and - 10 V \pm .01% applied to the 20 V span resistor (DUT pin 11) with relays K2 and K3 energized. BPOE includes the effects of unipolar zero offset current.

Prior to proceeding with this test the following conditions must be met or adjustments made to bring the voltages into tolerance

$$V_{REF} = + 10.000 \text{ V } \pm .01\%$$

$$\overline{V_{REF}} = -10.000 \text{ y } \pm .01\%$$

 E_0 = 0 ± 5 mV with all relays deenergized. If not, trim offset adjust pot. For E_0 = 0 ± 5 mV.

- (a) Set all DUT address inputs to "O"s and all Ref DAC address inputs to "1"s. Energize K7, K2, K3, and K4 in that order (K6 also if in CMOS mode) and measure V6 (adapter pin 21).
- (b) Set Ref DAC address inputs to 1111 1111 0001 and measure V_7 (adapter pin 21)

$$G_2 = 1 - \frac{(v_7 - v_6)}{(\frac{10}{4096})}$$
 [6-10]

(c) De-energize K4 and energize K7 and measure V8 (adapter pin 21).

$$BPOE = \frac{V_8}{G_2}$$

14. BPOE Drift

Repeat 13 for temperatures within the range of -55 to + 125°C and calculate $\Delta BPOE$ measured values shall be equal to or less than the values specified in Table I.

15. Power Supply Sensitvity Full Scale Due to $V_{\rm CC}$ (TTL).

With the DUT in the unipolar mode, K1, K2, and K5 energized, V_{CC} = + 5.0 V, and V_{EE} = - 15 VDC power supply sensitivity is tested.

(a) Set all DUT address inputs to logic "l"s and all Ref DAC address inputs to logic "O"s (outputs on).

$$\frac{E_o}{R_F/R_1} = V_{REF DAC} (FS) - I_o(FS)R_1 \text{ neglecting offsets}$$

or
$$I_o(FS)R_1 - V_{REF} DAC$$
 (FS) = $E_o(\frac{R_1}{R_F}) = \frac{E_o}{G_1}$ [6-11]

Ideally
$$E_0 = \frac{(R_1)}{R_F} = 0$$
 and $V_{REF DAC}$ (FS) = + 9.9976 = V_{DUT} (FS)

Varying the positive supply voltage, V_{cc} , by \pm 10% will cause E_{O} to vary by some ΔE_{O} .

The resulting values shall not exceed the limits specified in Table I.

(b) Set all DUT address inputs to logic "O"s and all REF DAC address inputs to logic "1"s (outputs off).

Varying the positive supply voltage, V_{cc} , by \pm 10% will cause E_o to change by some amount, ΔE_o .

+ PSS1 =
$$\begin{bmatrix} \text{change in DUT output} \\ \text{for 10% change in V}_{\text{cc}} \end{bmatrix} = \left| \frac{\Delta E_{\text{o}}}{G} \right| = \left| \frac{v_{13} - v_{12}}{G} \right|$$

or = $\left| \frac{v_{13} - v_{14}}{G} \right|$ [6-13]

The largest resulting value shall not exceed the limits specified in Table I.

The largest of the two errors (+ PSS1' or + PSS1") will be printed out and the conditions along with it. ($V_{\rm cc}$ & address)

16. Power Supply Sensitivity at Full Scale Due to V_{cc} (CMOS)

With the DUT in the Unipolar Mode, K1, K2, K5, and K6 energized, $V_{\rm CC}$ = + 15 V and $V_{\rm EE}$ = - 15 VDC power supply sensitivity is tested. Procedure is same as in 15, but with $V_{\rm CC}$ varied \pm 10%.

17. Power Supply Sensitivity at Full Scale Due to $V_{\rm EE}$ (CMOS)

With the DUT in the Unipolar Mode, K1, K2, K5, and K6, energized, $V_{\rm CC}$ = + 15 V, and $V_{\rm EE}$ = - 15 VDC power supply sensitivity is tested. Procedure is same as 15, but with $V_{\rm EE}$ varied \pm 10%.

18. Linearity

Some manufacturers use bit weight errors to determine the maximum positive and negative linearity errors with respect to a straight line between zero and full scale outputs. This method is valid for testing linearity if there is no appreciable bit interaction, thermal or other. Excessive bit interaction is apt to result in bit weight errors that are all in one direction. The maximum error would then seemingly occur at DUT input address of all ones. However, the DUT errors are calibrated to zero at full scale so the technique is not valid.

At this point in the test program development it appears that a vendor whose devices exhibit appreciable bit interaction would be required to test all 4095 outputs. The answer to this question and others will be a result of the characterization study.

As a part of this characterization the bit weight errors and corresponding linearity will be measured repetitively starting from initial turn on to acquire some data on the effects of thermal interaction on linearity measurement accuracy.

Linearity will also be measured for all 4095 codes after suitable warm up. A number of measurements will be made to check for repeatability.

1) Abbreviated Linearity Test Using Bit Weight Errors

Measure $E_{\rm O}$ and store for each of the following digital address inputs with same address applied to DUT and Reference Module:

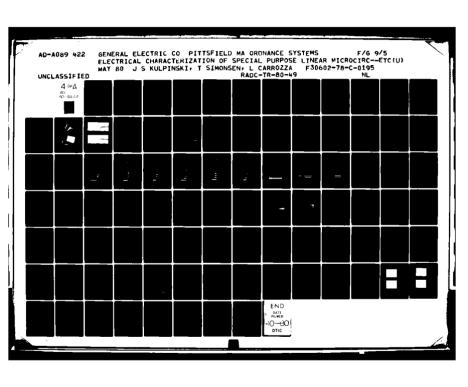
Establish a straight line with zero and full scale measured values. Calculate bit weight errors and derive addresses for both maximum positive bit weight error and maximum negative bit weight error.

All measured outputs for the above listed input addresses shall be linear to within \pm 1/2 LSB.

Apply the address for maximum positive bit errors and output shall be linear to within 1/2 LSB.

Apply the address for maximum negative bit errors and output shall be linear to within 1/2 LSB.

Subtract Pos. BWE from Neg. BWE store and record. Major Carry Errors (MCE) shall be less than \pm 0.9 LSB (-55 to \pm 125°C).



6.4.2 Monotonicity

One of the most important parameters of a D/A converter, if not the most important, is monotonicity. A D/A converter is monotonic if, for an increasing address (eg 0 - 4095), the output voltage/current continuously increases (or decreases if logic is complementary) and if, for a decreasing address eg (4095 - 0), the output voltage/current continuously decreases (or increases if logic is complementary).

The manufacturers recommending the abbreviated test method measure differential nonlinearity and claim that monotonicity is assured if the differential nonlinearity is \angle \pm 1 LSB. eg D.N.L. \angle \triangle E - LSBN LSBN

where LSBN is normalized LSB.

and $\triangle E$ is the value $E_{o(n)} - E_{o(n-1)}$

and $0 \le n \le 4095$.

Part of the characterization task will be to examine the validity of testing monotonicity via major carries.

Monotonicity will be tested by the following sequence:

- (a) Set. Ref. module and DUT addresses to all 0's and measure the error amplifier output voltage, $E_{O(0)}$.
- (b) Increment DUT address by one count and measure the error amplifier output voltage, $E_{O(0)}^{1}$. $E_{O(0)} = E_{O(0)}^{1}$ must be greater than 0 V.
- (c) Increment Ref. Module address by one count and measure $E_{o(1)}$. Then increment DUT address by one count and measure $E_{o(1)}^{1}$. $E_{o(1)}^{1}$ must be greater than 0 V.
- (d) Repeat for all 4095 addresses. If for all addresses $E_{o(n)} E_{o(n)}^{1} > 0$. The D/A converter (DUT) is monotonic.

NOTE: Linearity can also be measured at the same time without utilizing much memory.

Linearity - (All addresses)

Linearity can be measured along with monotonicity by first measuring the zero and full scale error voltages $E_{\rm O(0)}$ and $E_{\rm O(4095)}$, to establish a straight line and then measuring error voltages for all addresses in between relative to the straight line. Only max positive

and max negative deviations and respective addresses need be stored. However, for the purposes of characterization, the bit weight errors will be stored for comparison to BWEs measured in the abbreviated linearity test. After measuring linearity of all codes, repeat $E_{0(4095)}$ and $E_{0(0)}$. If $E_{0(4095)} - E_{0(0)}$ differs from the earlier measured values by $\frac{1}{2}.05$ LSB, repeat the sequence. If the latter condition is not met after two passes, stop the test, and indicate that DUT outputs are not stabilizing.

Appendix "A"

Linearity Equations

- VREF (m) = Ref. D/A output voltage at address "M".
- E_O (m) = Amplified difference voltage. Difference between Ref D/A and DUT output which includes offset voltage.
- E_O (0) = Amplified offset voltage which includes contributions from Ref D/A, DUT, and difference amplifier.
- VOI (m) = DUT output voltage on ideal straight line between zero and full scale for address "M". (referred to error amp. input)
- Vom (m) = Measured DUT output voltage for address "M". (referred to error amp. input)

and V_0 (DUT) = I_0 (DUT) R_1 (referred to error amp. input)

$$E_{o}$$
 (m) = I_{o} (m) $R_{1} + V_{REF}$ (m) G1
 V_{REF} (m) = $\frac{V_{REF}$ (FS) - V_{REF} (o)
 $\frac{4095}{}$ (o)

$$(V_{REF} (n) + I_{o} (n) R_{1}) G1 = E_{o} (n)$$

$$V_{OM}$$
 (m) 1 = I_o (n) $R_1 = \frac{E_o (n)}{G1} - V_{REF}$ (n)

$$v_{OI}(n) = (\frac{v_{OM}(FS) - v_{OM}(o)}{40.95}) n + v_{OM}(o)$$

where n is any address from 0 - 4095 and FS is 4095

6.5 Evaluation of Data

6.5.1 Dynamic Test Data

Settling time data was measured on 13 devices (Device Type 01) and the resulting data is listed in Table 6.2. Photographs were also taken and a typical set for a given device are shown in Figure 6.7. Settling time ranged from 400 to 600 nsec. The six devices supplied by Vendor "13" to GEOS with data (S/N, 4310 - 4315) exhibited settling times that were significantly less than the other devices tested, approximately 400 nsec settling time compared to 600 nsecs for the others. For all devices the "on to off" settling times were appreciably less than the "off to on" settling times, as much as 45% less for the slower devices and 30% less for the faster ones.

In the expanded photos shown in Fig. 6.7 there is some high frequency ac (damped) riding on the envelope of the signal. This ac is almost certainly a contribution from the test circuit, probably due to layout and wiring. The test circuit and the oscilloscope (plus preamplifier) employed appears to be adequate for testing device types 01. A sampling type preamplifier might be required to test device type 02s because of the lower settling times.

6.5.2 Static Test Data

Power Supply Currents

The supply current limits for the 562 appear to be adequate. I_{CC} seems to run towards the high side of the limits but it doesn't seem to change much from device to device.

Logic Input Currents

Devices tested seem to fall well within the limits specified. $I_{\rm TH}$ seems to increase randomly from one device to another at -55°C and occasionally over-ranges. This problem is almost certainly due to some slight condensation on the bottom of the DUT connector. Currents measured are low nano-amperes and should decrease at -55°C. Repeat tests on a sampling of devices has shown that it is not a device problem.

Logic "0" input currents ($I_{\rm IL}$) all measured well below the specified limits. Measured values were in the low nano-amperes range while specified limits are + 1 to - 200 uA.

Full Scale Current

Devices tested seemed to fall well within the limits specified. Limits specified are adquate.

Zero Scale Current

All devices passed these tests comfortably. Limits are reasonable.

Zero Current Drift

All devices passed these tests by good margins. Adequately specified limits.

Bipolar Offset Current

All devices passed this test with wide margins. This test is largely a measure of the bipolar offset resistor. If full scale output current is below nominal this resistor value will measure above nominal by almost the same amount. Although not tested directly the span resistor values will track the bipolar offset resistor values. It is because of this relationship between the resistance values and the F.S. output current value that the gain error is so low in spite of a \pm 25% tolerance on full scale output current.

Gain Error

All devices pass these tests with comfortable margins. Limits are adequate.

Gain Error Drift

Four devices failed this test over the range +25 to -55°C and six others came quite close to the limit. A couple of devices that failed measured slightly more than twice the limit specified. It should be noted that the maximum average temperature coefficient tabulated is not the average over the full temperature range but the worst case of the two averages over the temperature ranges of + 25 to + 125°C and + 25 to - 55°C. Averaging over the full operating temperature range would probably make the devices look better and some might even pass.

Bipolar Offset Error

All devices passed this test and it appears that this parameter is conservatively specified. It should be noted that the manufacturer sets the bipolar offset resistance 50 ohms low to allow for the insertion of a 100 Ω potentiometer in series with the resistor to adjust bipolar offset error to zero if so desired. A 50 Ω resistor was inserted in series with the bipolar offset resistor for this test to achieve nominal value.

Bipolar Offset Drift

All devices passed this test, most by a comfortable margin, but from $+25^{\circ}\text{C}$ to -55°C . A couple of devices came to within approximately 50% of the specified limit.

Power Supply Sensitivity

Power supply sensitivity was tested for CMOS and TTL operation with all bits on and with all bits off. CMOS power supply sensitivities were tested at $V_{\rm cc}$ = +5 V and $V_{\rm cc}$ = +15 V. Measured values of output voltage variation were in no case greater than ± 100 uV with ± 10% supply voltage variations. This parameter appears to be ultra conservatively specified, especially for $V_{\rm EE}$. It would appear that a ± 500 uV limit for all supplies would suffice over the full operating temperature range.

Bit Weight Errors

All devices tested passed the Bit Weight Errors (BWE) tests. BWEs were generally quite low at $+25^{\circ}$ C. At $+125^{\circ}$ C BWE degraded slightly but the most significant changes occurred at -55° C. It appears that the manufacturers do their screening at $+25^{\circ}$ C and select devices with low bit errors to allow a safe margin for variation at -55° C. Figures 6.8 - 6.10 and Figures 6.14 - 6.16 illustrate this feature.

It is interesting to note that there seems to be a recurring pattern to the Bit Weight Errors and Major Carry Errors, as shown in Figures 6.8 - 6.13. The current switches in this device are identical quads with scaling resistors at the outputs of the two lower order quads. The recurring pattern seems to reflect scaling resistor errors and drifts.

The Bit Weight Errors measured in the "Abbreviated Linearity Test" correlated quite well with the Bit Weight Errors extracted during the extended linearity test. Some of the differences noted, however small, were probably related to temperature stabilization time, especially at - 55°C. Bit Weight Errors and Major Carry Errors for both the abbreviated and extended linearity tests are displayed side by side for comparison.

Summation Bit Weight Errors

The accuracy of the summation of (+) Bit Weight Errors and the summation of (-) Bit Weight Errors in defining the worst case positive and negative linearity errors respectively is dependent upon how much interactive error is present in the device. The devices

tested exhibited very little interactive error, as demonstrated by the low values of \sum (+) NL + \sum (-) NL. Typically the values were ∠ ± .05 LSB. Confirmation of the low interactive errors was achieved by the close correlation of the Extended Linearity Test data with the Abbreviated Linearity Test data. In the extended test all codes were tested and the addresses of the maximum positive and maximum negative linearity errors were recorded. Although the addresses of the maximum positive error and the maximum negative error were not always exact complements, the \sum (+) NL + \sum (-) NL were always within 0.1 LSB. The smaller the bit errors the more unpredictable the addresses will be. Better correlation would be achieved if all bits with measured bit weight errors of \angle ± .05 LSB were weighted as logic "0"s. Figures 6.8 - 6.10 illustrate Bit Weight errors for abbreviated and the extended tests and the addresses of the worst case positive and negative linearity errors for each test are tabulated below the graph. Extended Linearity test data is not listed in Table III. It only shows up in the data plots for comparison purposes.

Major Carry Errors

Major Carry Errors were generally well within the specified limits of \pm 0.9 LSB in the abbreviated test. Although monotonicity is tested accurately for all codes in the extended tests, major carry errors were extracted from the extended test data for comparison to the abbreviated test data. Comparisons were good as shown in typical device MCE graphs in Figures 6.11 - 6.13.

6.6 Conclusions and Recommendations

The characterization of the 562 was successful in accomplishing all of its primary objectives. Although only one Device Type (01) made by only one vendor was characterized, its performance over the full military operating temperature range was evaluated and it performed well. Twelve devices doesn't constitute a large sample but it's enough to indicate potentially sensitive parameters. The only parameter that appeared to be marginal was gain error drift with temperature. 5 ppw/°C is not large enough. The limits should be increased to 10 ppw/°C at the least. Generally, parameter tolerances tended to be conservative. Logic "O" Input Current appears to be much too loosely specified. None of the values measured were in excess of ± 20 nA, yet the specified limits are $+1 \longrightarrow -200$ mA. It is recommended that the limits be reduced to + 1 \longrightarrow - 200 nA. Another parameter that appeared to be much too conservatively specified was Power Supply Sensitivity. Generally, the output variations in response to ± 10% power supply variations were less than ± 100 mV and in no case did they exceed ± 200 uV over the full operating temperature range. Also, the sensitivity to the negative power supply was no worse than to the positive. It is recommended, therefore, that one limit be applied to both the positive and negative power supplies over the full temperature range, ± 800 uV. Linearity was good and superposition (interactive) errors were extremely low, ∠± .05 LSB. The device tested is an excellent candidate for performing "Abbreviated Linearity Testing" since the device is linear and superposition applies. A device that is not linear and exhibits interactive errors that should be compelled to perform "All Codes Linearity Testing," unfortunately devices of this nature were not available for characterization. Nevertheless, anticipating that such devices will eventually be tested, the following recommendations are offered:

- 1. Devices that exhibit low interactive errors ($\sum + NL + \sum NL \le 0.1$ LSB) be permitted to perform "Abbreviated Linearity Tests" while those that do not must perform all codes testing.
- 2. The device slash sheets be modified to include at least one and possibly two more interactive error tests at half scale and three quarters full scale. e.g.

0111 1111 1111 + 1000 0000 0000 0.1 LSB and 0100 0000 0000 + 1011 1111 1111 0.1 LSB

Without the inclusion of one or both of the latter tests a device with interactive errors in excess of \pm 0.1 LSB but whose bit weight errors each are \angle 0.5 LSB could pass the "Abbreviated Linearity Test". If all bit errors are negative the address of Σ - NL would

be all 1s and the address of Σ + NL would be all 0's. Both of the latter addresses are calibration points on the ideal linearity curve so Σ + NL + Ξ - NL = 0.

Some vendors have suggested walking a zero through the test pattern but that is not as effective as the proposed two tests. Addition of the walking zero codes, if implemented, should be in addition to the proposed test addition.

Another recommendation pertaining to guaranteed monotonicity is to apply a \pm 0.9 LSB limit to Major Carry Errors in the "Abbreviated Linearity Test" to allow for measurement error and interactive errors, however slight, that could make a marginally non-monotonic device appear to be monotonic or vice versa. Failure to meet this requirement would not necessarily constitute a device failure. If MCE is in the range of 0.9 LSB \leq MCE \leq 1.1 LSB the device must be subjected to "All Codes Linearity Test" in which monotonicity is more accurately tested for all codes. Inability to pass this test would constitute a failure.

Settling time measurements appeared to be valid but without the manufacturer's test data the results could not be correlated. Results appear to be significantly better than manufacturers indicated they would be.

Another objective of the 562 characterization effort was the development of automatic test capability for testing the device on a Tektronix S3260. This was made possible by the use of a Reference Module which contains an 18 Bit Reference DAC, buffers, and active ground drivers. A Fluke 8500A (5 1/2 Digit DVM) was employed via IEEE bus simply to calibrate the test setup at the start of testing. Once calibration is done it is not repeated for subsequent DUT testing. The accuracy of the tester is excellent and so was correlation with manufacturer's 25°C test data on devices S/Ns 4310 -4315. Correlation was within ± .05 LSB.

	I					vice		1
	!	Conditions:	-		limits		limite	4
Characteristics	Symbol	<u> </u>		Min	Max	Min	Max	Units
Supply Current]]					Ι.
from Vcc	Icc	All input bits logic "1"		3_	18	3	18	mA
Supply Current	١.	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- 1	25	١ .		ن ا	{_ .
from Vee	Iee	All input bits logic "1"		-25	-5	-40	5	mA
Logic "1" Input	1	Vin (Logic "1") = + 15 V, Each		- 1	+100	- 1	+100	
Current	IIH	input measured separately		- 1	7100		7100	JUN .
Logic "0" Input	}	Vin (Logic "0") = 0 V, Each	J			ĺ		l
Current	IIL	input measured separately	- 1	-200	-1	-200	+1	μA
Full Scale	 	All inputs logic "1"	11			 	_	
Current	IFS	Vo = 0 V	_	-2.5	-1.5	-6	-4	mà
Zero Scale	 	All inputs logic "O"			 	 	1	
Current (TTL)	Izsi	Vo = 0 V, Vcc = + 5 V, TA = +25°C	ļ	05	+.05	05	+.05	% 7S Cur: :r
Zero Scale	-231	All inputs logic "0"			 	 -	-	% FS
Current (CMOS)	IZS2	V _O = 0 V, V _{CC} = +15 V, T _A = +25°C	- (05	+.05	05	+.05	Currer
) - 530	I	. i		1.00			
Zero Scale	Δ Izs/	All inputs logic "0"						PPM /
Drift	/ _{AT}	Vcc = + 15 V		-2	+2	-2	+2	IFS/C
Bipolar Offset	Τ							I
Current	IBIP			0.75	1.25	2	3	mΑ
Gain Error	V	All inputs logic "1" V _{FSI} = V ₀ - 9.99756	1		1)	į	!
(TTL)	FS I 1							l
 	ļ	Vcc = + 5 V, T _A = + 25°C All inputs logic "1"		-25	+25	-25	+25	mv
Gain Error	V _{FS I2}	VFS1 = Vo - 9.99756			Ì	1	!	
(CMOS)	1512	Vcc = + 15 V	i	-25	+25	25	- 725	_
Gain Error	No. 7	All inputs logic "1"	—		123	1 -25		DDM
Drift	AVFSI	Vcc =		-5	+5	-5	+5	VFS/C
Bipolar	744	Bit 1 = logic "1"			-	 	,	
Offset Error	BPOE	Bits 2 - 12 = logic "0"			1		:	1
	3.00	Measure $V_0 - 0 V$ $T_A = +25$ °C		-20	+20	20	+20	m∨
Bipolar		All inputs logic "O"				\Box		
Offset Error	△ BPOE		}			1	1	PPM / VFS/C
Drift		Measure Δ^{V_0}		-4	+4	-4	-4	VFS/C
Power Supply		Vcc = + 5 V ± 0.5 V	Ę		ļ		i —	
Sensitivity			1		}	1	1	
At Full Scale	+PSS1	$T_A = \pm .25^{\circ}C$	4	-800	+806	800	+800	٧٧
From Vcc					l	1		
(TTL)		$T_A = -55 \text{ to} + 125^{\circ}\text{C}$ $Vcc = +15 \text{ V} \pm 1.5 \text{ V}$	<u></u> ì	-1.6	+1.6	-1.6	+1.6	mV_
Power Supply	Į.	Vcc = + 15 V ± 1.5 V	12		1	[!	
Sensitivity		T _A = + 25°C]	200	1,000		1,000	
At Full Scale	+PSS2	A + + 25°C	1	-800	+800	-800	+800	μ۷
From Vcc	1	T	ĺ		1 49 6	1	اريدا	
(CMOS)	l	$T_A = -55 \text{ to} + 125^{\circ}\text{C}$		-1.6	T1.0	-1.ó	TLO	MΑ

		ble 6.1 Electrical Performance Character	1		evice		
		Conditions: See Note 3	01	limits	02	limits	1
Characteristics	Symbol		Min	Max	Min	Max	Units
Power Supply		V _{EE} = - 15 V ± 1.5 V					1
Sensitivity		All inputs logic "1" TA = + 25°C	-1.6	+1.6	-1.6	+1.6	mV
At Full Scale	-PSS1		í				
From VEE		, m	ì	1			l
		$T_{A} = -55 \text{ to } + 125^{\circ}\text{C}$	-3.2	+3.2	-3.2	+3.2	mV
Bit Errors	B1 - B12	Turn on 1 bit at a time and measure L2	;				
		Vo relative to REF. DAC output.		1			ł
		$T_{A} = -55 \text{ to} + 125^{\circ}\text{C}$	-1.22	+1.22	-1.22	+1.22	mV
Summation of		Turn on all bits with Positive bit 13	,			- 4	
Positive Bit	_	errors and measure Vo relative to		i i			1
leight Errors	\sum (+) BWE	REF. DAC TA = - 55 to + 125°C	-1.22	+1.22	-1.22	+1,22	mV
Summation of		Turn on all bits with Negative bit 11					
Negative Bit		errors and measure Vo relative to		1 :			ì
eight Errors	∑(-) BWE	REF. DAC TA = - 55 to + 125°C	-1.22	+1.22	-1.22	+1.22	mV
iajor Carry	MC1 - MC11		,				
Errors			}				
	_	$T_A = -55 \text{ to } + 125^{\circ}\text{C}$	-2.2	+2.2	-2.2	+2.2	mV
Output Current		All inputs switched simultaneously.					
Settling Time	tSLH	Time to settle to within 1/2 LSB of		[]			
to FS	J.111	final value	-	1		0.4	µ8 ес
Output Current		All inputs switched simultaneously.					
Settling Time	t _{SHL}	Time to settle to within 1/2 LSB of					
7S to 0		final value	•	1		0.4	μsec
Bit	(+) BWE						
Interaction	+ (-) BWE] ,	-0.25	+0.25	-0.25	+0.25	- V

- Notes: 1. The compliance voltage range varies from one vendor to another. Devices with a finite output resistance will draw additional current proportional to compliance voltage. eg. If R_O = 6 K A. and compliance voltage equals + 1 V the output current will increase by 0.167 mA. This current is a fixed offset current. This device is not a multiplying DAC.
 - This test is performed in the unipolar mode over a 0 to + 10 V range. One LSB is 2.44 mV.
 - 3. The operating temperature range is 55 to 125°C unless otherwise stated. Vcc = + 15 \pm .15 V VEE = 15 \pm .15 V

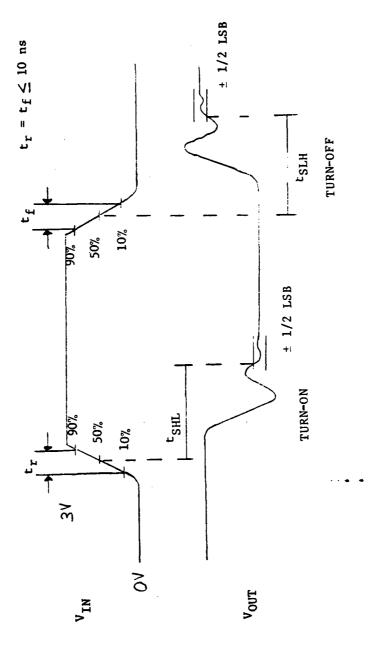


Figure 6.3. Waveforms For Settling Time, Device Types 01 and 02.

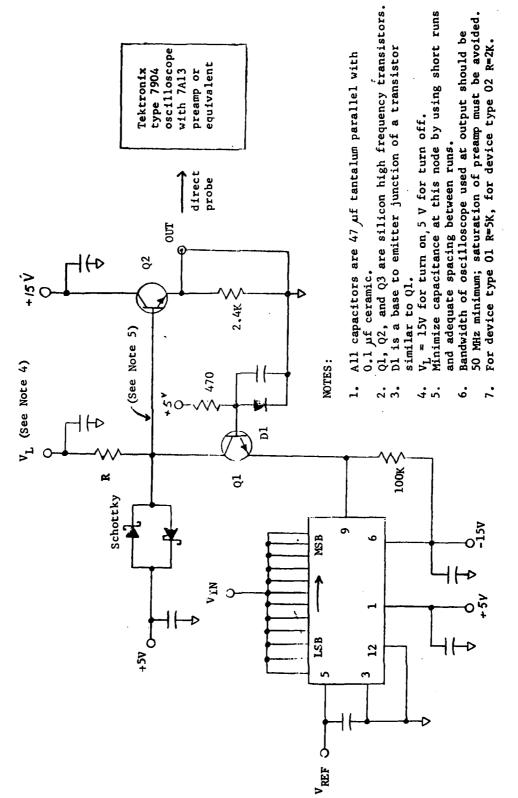


Figure 6.4. Test Circuit For Settling Time, Device Types 01 and 02.

VI-36

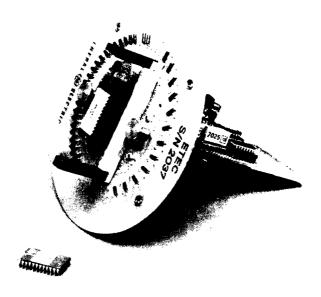


Figure 6.5. S3260 test adapter for the 562, D/A Converter.

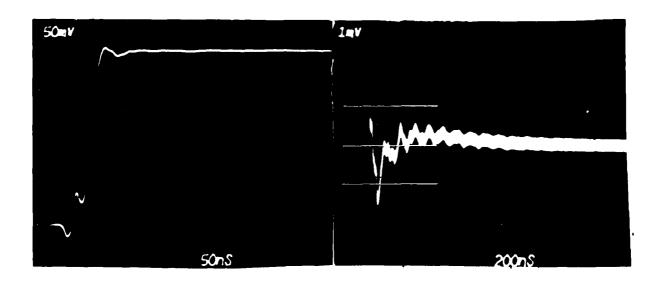


Figure 6.6. Reference module connected to the S3260 test adapter.

50ns Inv

0-1 Transition Overall (a)

0-1 Transition Expanded (b)



1-0 Transition Overall (c)

1-0 Transition Expanded (d)

Figure 6.7. Settling time waveforms (typical device type 01). VI-38

TABLE 6.2. Output Settling Time Data

Device Type 01

Serial Number of Device	All Bits Off to All Bits On	All Bits On to All Bits Off
00005	500 ns	260 ns
00019	480 ns	300 ns
00020	500 ns	260 ns
00021	480 ns	260 ns
00025	480 ns	220 ns
00035	480 ns	360 ns
00048	480 ns	245 ns
04310	400 ns	290 ns
04311	370 ns	240 ns
04312	360 ns	240 ns
04313	370 ns	245 ns
04314	380 ns	245 ns
04315	400 ns	240 ns

TABLE 5.3. Device Type 01 Data at + 25°C.

		HI-LIM CMITS 18:0 % -6:00 M		223 8888888888		**	2.00 PPH.	6. 33 6. 33 6. 33	1.68x 58x 58x 58x 58x 58x 58x 58x 58x 58x 5	######################################
	×	12.7	2222222300000 222222223000000		0.00 0.00	• 4	•	-77.	-77.0	
	=	13.1			2.00	-95.0	: :	- 20.7 - 10.03	-24.8 50.7	######################################
	2	27.	######################################		9.5	-97.5 -123.	. 60	10.3	-5.14	######################################
~	ë		#~#~~~~~##############################		2.17 2.18	-1 08 . -122.	9 9	-13.9	-27.5	64448-198-1-49
10.58.01	•	 	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	· · · · · · · · · · · · · · · · · · ·	8 8 8 8 8 8	-72.0 -114.	3 :	-78.6 52.4		TEREFERENCE CO
88 OCT 79	4316	11.0			1.91	-41.0 -85.0	96.90	26.6	-6.19 15.6	0140-4-4-4-4-4-4-4-4-4-4-4-4-4-4-4-4-4-4
DEG C 1 1	+31+			$\begin{array}{cccccccccccccccccccccccccccccccccccc$	1.93	-31.5	6.00 E.000	-15.4	-1.0 80.6	448-8448844 F
TENFERATURE: 28	4313	- 22	# # # # # # # # # # # # # # #	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1.92	-38.6 -68.5	99.90	-31.8	5.21 80.21	
-	4318		~~************************************		9.5	-23.5 -60.5	0.00 075.3	-66.6	15.4	0
VPE: 882,	+310	-15.0	######################################		1.93	-58.0	6.90 975.F		-82.7	ELECTRICATE A
DEVICE TO	,		***********	**************************************	1.50	-1.00K	-2.00	***	-1.60K -1.60K	ETETETETETE
1 1300 H34		CURRENT		######################################	CURRTTL CURRCMOS	CURRTTL CURRCHOS	FSET CURR.	(CNOS) [+16X] (CNOS) [-16X]	C-1043	
HON-JFACT JRER	PARATETER	ICC-BUPPLY IEE-SUPPLY		III FOR BEILL FO	FULL SCALE FULL SCALE	ZERO SCALE ZERO SCALE	102-DRIFT C BIPOLAR OFFSET CURI	+PSS2 (CNO+PSS2 (CNO	-P\$\$1 (TTL)	######################################

TABLE 6.3. Device Type 01 Data at + 25°C.

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-EMPERATURE:	4 6.1.		6.66 N 2 S 2 S 2 S 2 S 2 S 2 S 2 S 2 S 2 S 2	1.99		55. 45.	10 10 10 10 10 10 10 10 10 10 10 10 10 1
TVPE: 668,	N 90	**********		00 v.		- 56	### 44565 ##############################
DEVICE TVP	10-L3	***********	**************************************	90 90	2	E	
MANUFACTURER CODE: 1 DE	PARAMETER ICC-SUPPLY CURRENT IEE-SUPPLY CURRENT		III FOR BITTS 1 III FOR BITTS 2 III FOR BITTS 4 III FOR BITTS 6 III FOR BITTS 6 III FOR BITTS 9 III FOR BITTS 10 III FOR BITTS 10 III FOR BITTS 11	FULL SCALE CURRTTL FULL SCALE CURRCHOS ZERO SCALE CURRTTL	SCALE CURR.	CCHOS) [Passing Carlot C

TABLE 6.3. Device Type 01 Data at + 25°C.

MANUFACTURER CODE: J DEVICE TYPE: BGE, TEMPERATURE: 85 DEG C J 25 OCT 79 10:58:45

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		žž.	8.	2	÷ \$		
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=	233.8 17.88	4.15	:	-3.20		-104. 49.6	255.3 255.3 255.3 25.3.6 25.3.6 25.3.6 25.3.7 25.3.7
2	186.7 -261.7 -16.47	** **	•	-722.R	•	-113.	200 200 200 200 200 200 200 200 200 200
•	104.8	##. 1.18	•	-4.59	•	-68. • 8.	6.10 1.00
•	166.7 -154.7 11.67	6.83	•	-3.57	•	-78.6 30.6	4
4316	- 100-72 - 100-72 - 100-72	7.7. 7.7.	•	-3.43		-31.0	40.00 40
16	E. 200.11		•	-4.16		6.6 6.6 6.6	1.00.00 1.00.0
4313	100.17 100.17 100.17	-861.M -1.02	•	H.167-		-78.1	21.00.00.00.00.00.00.00.00.00.00.00.00.00
4318	144 144 148	77.7	•	-3.40		-97.4	45.11 48.47.14 48.47.17.17.17.17.17.17.17.17.17.17.17.17.17
916	828 828	7.7 7.7	:	-2.7	:	-165. 87.8	6.82.22.25.69 2.22.25.23.25.59 2.22.25.23.25.25.25.25.25.25.25.25.25.25.25.25.25.
L0-L1M	233 233 247		-5.8	-20.0	2.7	**	
PARANETER	SUM BIT ERROR(+) SUM BIT ERROR(-) SUM-ERROR(+)+ERROR(-)	GAIN ERROR (17L) GAIN ERROR (CNOS)	GAIN ERROR DRIFT (TTL)	BIPOLAR OFFSET ERROR	PPOE DRIFT		RUR CARRY ERR-BITS 2 RUR CARRY ERR-BITS 2 RUR CARRY ERR-BITS 5 RUR CARRY ERR-BITS 5 RUR CARRY ERR-BITS 5 RUR CARRY ERR-BITS 6 RUR CARRY ERR-BITS 8 RUR CARRY ERR-BITS 8 RUR CARRY ERR-BITS 8 RUR CARRY ERR-BITS 8 RUR CARRY ERR-BITS 9 RUR CARRY ERR-BITS 11

TABLE 6.3, Device Type 01 Data at + 25°C.

MANUFACTURER CODE: 1 B	DEUICE TYPE: SER,	PE: 562,	TEMPERA		TEMPERATURE: 26 DEG C , 25 OCT	16 OCT 1	5	10.58.59
PARATER	LO-LIM	×	4					
SUM BIT ERROR(+) SUM BIT ERROR(-) SUM-ERROR(+)+ERROR(-)	### ####	EEE	* * * * * * * * * * * * * * * * * * *	2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 3 3 3 3	E 333			
GAIN ERROR (TTL) GAIN ERROR (CHOS)	## •••	3.63 9.17	## ##	zz	55			
GAIN ERROR DRIFT (TTL)	-5.8			8.	PPH/C			
SIPOLAR OFFSET ERROR	-20.0	-2.11	-3.12	ž	£			
PPOE DRIFT	• •	:	:	\$	PPH/C			
+PSS1 (TTL) [+10%] +PSS1 (TTL) [-10%]	-808	-43.6	-20.1		3 3			
ALR CARRY ERR-BITS 1 ALR CARRY ERR-BITS 2 ALR CARRY ERR-BITS 4 ALR CARRY ERR-BITS 5 ALR CARRY ERR-BITS 5 ALR CARRY ERR-BITS 6 ALR CARRY ERR-BITS 6 ALR CARRY ERR-BITS 6 ALR CARRY ERR-BITS 6 ALR CARRY ERR-BITS 9 ALR CARRY ERR-BITS 9 ALR CARRY ERR-BITS 9			44884 4488 4488 44884 44884 44884 44884 44884 44884 44884 44884 44884 44					
		:		•				

TABLE 6.4. Device Type 01 Data at + 125°C.

NANUFACTURE CODE: , DEVICE TYPE: 802, TEMPERATURE: 185 DEG C , 85 OCT 79

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ä	-0.	######################################		2.01 2.02	59.0 48.5	179.8	96.7	39.7	
	•				717			7	
2	3.2 6.7		86.6.6.6.6.6.6.6.6.6.6.6.6.6.6.6.6.6.6.	1.95	44.5 69.0	273.R	20.5 51.3	35.9	**************************************
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2	15.4	**************************************	######################################	2.18 2.18	48.0	428.	-68.6 -41.2	73.2	
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	====	577.450 my 07. 30		ALA)	16.0 -30.5	385.	-30.4 -65.2	-91	1.00 A 0.
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TABLE 6.4. Device Type 01 Data at 125°C.

1; 186133

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že č Št	1111111111	\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$\$	44 44 EE 22	PPA/C	33 33	52222222
H1-L13		••••••••••••••••••••••••••••••••••••••	2.5 2.5 4.5 4.5 4.5 4.5 5.5 6.5 6.5 6.5 6.5 6.5 6.5 6.5 6.5 6	2.8		
4	00-0000me.		2.09 1.09 -97.0	185.M		- nuonom
36	######################################	######################################	2.69 2.69 -14.6	385.M 1.05		. 86446 .6 .6
10-13 3.00-	•••••••		1.59 1.59 1.00 1.00 1.00 1.00 1.00 1.00 1.00 1.0	-2.00 750.M		
PARAMETER 10C-SUPPLY CURRENT 1EE-SUPPLY CURRENT		III FOR BITS 1 III FOR BITS 2 III FOR BITS 3 III FOR BITS 4 III FOR BITS 4 III FOR BITS 7 III FOR BITS 9 III FOR BITS 10 III FOR BITS 11 III FOR BITS 11 III FOR BITS 11	FULL SCALE CURRTTL FULL SCALE CURRCMOS ZERO SCALE CURRTTL ZERO SCALE CURRCMOS	IOZ-DRIFT Bipolar offset curr.	+PSS2 (CMOS) [+1043] +PSS2 (CMOS) [-1043] -PSS1 (TTL) [-1043]	

NOTES:1.2ERO (8) IN LIMITS COLUMN SEANS NO LIMIT. IT CAN BE INTERPRETED AS A DASH (-).

TABLE 6.4. Device Type 01 Data at + 125°C.

MANUFACTURER CODE: J. DEUICE TYPE: 562, TEMPERATURE: 185 DEG C. J. 25 OCT 79 PARARETER

11:06:63

	333	55	È	£	È	33	123 123	123	151	125	123 123 123
		zz ::	8.8	%	*		23			8	
	1.85. 1.85.										
=		 ##	-1.12	-3.17	15.84	-124.	207.H	257.R	-2.34	, 34 1	-26.7H
2	-99.73 -7.63	4.0 9.0 4.0 4.0	-546.M		361.R	-133.	310.H	151.A	-17.01	9	-10.94 -25.64
9	22.13	4.583	-3.53	-5.46	-439.N	4.57	-255.M 211.M	175.H	50.05 F. 0.05	45.6F	-4.21A
•	-275.3 21.33	6.30 6.18	-1.44	-5.06	-745.R	-17.4	-337.R	140. H	-64.6A	-57.5M	
4315	2000 1000 1000 1000 1000 1000 1000 1000	-36.81	1.14	-3.8	217.N	-51.7	52.94 114.8	116.H	25.4	-10.64	16.94 16.94
+10+	 600. 6.60.		538.H	-3.45	367.H	-165. 103.	E. E. S.	258.E	-52.52 FR. 52		18.00 18.00
4313	2000 2000 2000 2000 2000 2000 2000 200	200 200 200 200 200 200 200 200 200 200	-103,N	-625.N	52.8H	-119. -15.5	4 4	183.5	-4.15H		
4318		## ## ## ## ## ## ## ## ## ## ## ## ##	 \$	-2.67	363.R	25.5 36.5 36.5	259.H	176.H	-27.4 -27.4	6.308	23.17 -19.01
4310	2.00 6.00 6.00 6.00 6.00 6.00 6.00 6.00	35	3.1	-3.10	-196.8	 	74.7H	207.E	2.39H	12.94	34.9H
10-11M	333	žķ.	-5.8	-20.0	8 .7	**	60 60 60 60 60 60 60 60 60 60 60 60 60 6			E E I	E E E
	SUM BIT ERROR(+) SUM BIT ERROR(-) SUM-ERROR(+)+ERROR(-)	GAIN ERROR (TTL) GAIN ERROR (CHOS)	GAIN ERROR DRIFT (TTL)	BIPOLAR OFFSET ERROR	BPOE DRIFT	+PSS1 (TTL) [+1013 +PSS1 (TTL) [-1013	HUR CARRY ERR-BITS 2	MUR CARRY ERR-BITS 3	MUR CARRY ERR-9118 5	FLOR CARRY FRE-WITE SE	FUR CARRY ERR-BITS 10 FUR CARRY ERR-BITS 10 FUR CARRY ERR-BITS 11

TABLE 6.4. Device Type 01 Data at + 125°C.

### ### #### #########################				•	1		
TERROR(+)	PARANETER						
TERROR(+) -800.R 114.H 196.R		L0-L1M	*	#		•	
ERROR (TTL) ERROR (CNOS) AR OFFSET ERROR -26.0 -3.12 -1.18 5.00 AR OFFSET ERROR -4.06 -715.M -395.M 4.00 (TTL) [+19M] ARRY ERR-BITE 2 -906.M 111.M 275.M 990.M 48RY ERR-BITE 3 -906.M 111.M 275.M 990.M 48RY ERR-BITE 3 -906.M -23.M 130.M 990.M 48RY ERR-BITE 5 -906.M -7.79 130.M 990.M 48RY ERR-BITE 5 -906.M -7.79 130.M 990.M 48RY ERR-BITE 5 -906.M -7.79 130.M 990.M 48RY ERR-BITE 5 -906.M -7.79 130.M 990.M 48RY ERR-BITE 5 -906.M -7.79 130.M 990.M 48RY ERR-BITE 5 -906.M -7.79 130.M 990.M 48RY ERR-BITE 6 -906.M -7.79 130.M 990.M 48RY ERR-BITE 8 -906.M -7.79 130.M 990.M 48RY ERR-BITE 8 -906.M -7.79 130.M 990.M 48RY ERR-BITE 19 -906.M -7.79 17.70 990.M 48RY ERR-BITE 19 -906.M -7.79 17.70 990.M 48RY ERR-BITE 19 -906.M -7.79 17.70 990.M 48RY ERR-BITE 19 -906.M -7.79 17.70 990.M 48RY ERR-BITE 11 -906.M -3.92 M -49.6M 990.M 48RY ERR-BITE 11 -906.M -3.5.1M -49.6M 990.M 990.M 48RY ERR-BITE 11 -906.M -3.5.1M -49.6M 990.	9UF BIT ERROR(+) 9UF BIT ERROR(-) 9UF-ERROR(-)	333	• •		***	999	
ERROR DRIFT (TTL) -5.00 -3.12 -1.18 5.00 AR OFFSET ERROR -20.0 -3.54 -3.91 20.0 ORIFT -4.00 -715.M -395.M 4.00 (TTL) [-10M] -80051.9 10.0 800.N ARRY ERR-BITE 2 -900.M -131.M 235.M 900.M ARRY ERR-BITE 3 -900.M -48.8M 141.M 900.M ARRY ERR-BITE 5 -900.M -7.3M 130.M 900.M ARRY ERR-BITE 5 -900.M -7.3M 130.M 900.M ARRY ERR-BITE 5 -900.M -7.3M 130.M 900.M ARRY ERR-BITE 5 -900.M -7.3M 130.M 900.M ARRY ERR-BITE 5 -900.M -7.3M 130.M 900.M ARRY ERR-BITE 5 -900.M -7.3M 130.M 900.M ARRY ERR-BITE 6 -900.M -7.3M 122.7M 900.M ARRY ERR-BITE 10 -900.M -7.3M -22.3M 900.M ARRY ERR-BITE 11 -900.M -7.3M -22.3M 900.M -7.3M -7.2M -7.	GAIN ERROR (TTL) GAIN ERROR (CNOS)	zz 	41.4.E	 	zz ::	22	
	GAIN EPROR DRIFT (TTL)	-5.8	-3.12	-1.18	2	PPR/C	
TTL) [+10%] -80061.9 -100. 800. TTL) [+10%] -8009.53 10.0 800. TTL) [-10%] -8009.53 10.0 800. TTL) [-10%] -8009.53 10.0 800. TTL) [-10%] -8009.53 10.0 800. TTL) [-10%] -9009.53 10.0 800. TTL] -10%] -9009.53 10.0 900. TTL] -10%] -9009.53 10.0 900. TTL] -10%] -9009.50 10.0 900. TTL] -10%] -900. TTL] -10%] -	BIPOLAR OFFSET ERROR	-20.0	-3.54	-3.91	8	35	
TTL) [+10%] -89051.9 -100. 800. TTL) [-10%] -8009.53 10.0 800. RV ERR-BITS -900. 111. 379. 900. RV ERR-BITS -900. -40.81 141. 900. RV ERR-BITS -900. -40.81 130. 900. RV ERR-BITS -900. -7.34 130. 900. RV ERR-BITS -900. RV ERR-BIT	BPOE DRIFT	4 .4.	-715.H	-385.R	÷	PPR/C	
CARRY ERR-BITE 1 -900.M 111.M 379.M 900.M CARRY ERR-BITE 2 -900.M -131.M 225.M 900.M CARRY ERR-BITE 3 -900.M -131.M 235.M 900.M CARRY ERR-BITE 5 -900.M 97.4M 7.84M 900.M CARRY ERR-BITE 5 -900.M 7.79M -362.M 900.M CARRY ERR-BITE 8 -900.M 7.79M -12.7M 900.M CARRY ERR-BITE 9 -900.M 7.79M -12.7M 900.M CARRY ERR-BITE 9 -900.M 7.79M -12.7M 900.M CARRY ERR-BITE 9 -900.M 7.79M -12.7M 900.M CARRY ERR-BITE 1 -900.M 7.79M -12.7M 900.M CARRY ERR-BITE 1 -900.M 7.79M -12.7M 900.M CARRY ERR-BITE 1 -900.M 7.79M -12.7M 900.M 00	+PSS1 (TTL) [+10%] +PSS1 (TTL) [-10%]	÷	-61.9	; . ; .		33	
CARRY ERR-BITS 4 -900.N -23.4N 139.N 900.N CARRY ERR-BITS 5 -900.N 27.3H 7.84N 900.N CARRY ERR-BITS 7 -900.N 7.79N -362.U 900.N CARRY ERR-BITS 9 -900.N 7.79N -12.7N 900.N CARRY ERR-BITS 9 -900.N 7.79N -22.9N 900.N CARRY ERR-BITS 9 -900.N 7.79N -22.9N 900.N CARRY ERR-BITS 1 -900.N -3.92N -12.7N 900.N CARRY ERR-BITS 1 -900.N -3.53.N -49.6N 900.N	CARRY CARRY		111.E	379.9 235.9	E.E.E.		
CARRY ERR-Bils b - 900-H 7.79H - 362-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H - 562-U 900-H 7.79H 900-H	CARRY ERR-BITS	E.E.	-83.48 9.748	1 39.7 7.843			
CERRY EXX-BITS 10 -906.N -3.92N -12.7N 906.N CARY EXX-BITS 11 -966.N -35.1N -49.6N 906.N	CARRY ERR-BITE CARRY ERR-BITE CARRY ERR-BITE			36.5. 2.5.5. 2.4.4.	000 000 000 000		
	CARRY ERR-BITS CARRY ERR-BITS	000		-12.7H	E. 000		

TABLE 6.5. Device Type 01 Data at - 55°C. NANUFACTURER CODE: J BEVICE TYPE: SER, TEMPERATURE: -SS DEG C , 86 OCT 79

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	E		***********	8.5 8.5	 \$ \$	8.8	1	 		
1	12.0	44444848486644 6648887-6446	######################################	2. S. S. S. S. S. S. S. S. S. S. S. S. S.	6.00	5.678	-127.	-13.6		
ì	7.0 7.0		2 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	. v. v.	-1 0 1. -138.	-40.47	4.4 9.0	2.5 2.0		
8	2.0	######################################		1.94	-132.	-226.H	. a m	-114. 67.8	200111011102 400111011102 400111011102 5001101110110110110110110110110110110110	
:			2.00 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	2.17	-124.	-94.87	-73.5	-9.19	######################################	
			######################################	8.28 7.29	-136.	-347.8		**	4 - 4 - 1	C-) HEND
4.5	, a.e.			1.92	-53.0	-78.34 8.34	31.8	-15.6 46.8	PW90-07-400-6	MPRETED AS A
	10.7			1.93	-54.5	-149.H	-124. 51.8			NE INTERPR
,,,,		22-6-4-4-4-4-4-4-4-4-4-4-4-4-4-4-4-4-4-4	**************************************	1.92	-53. 0	187.78	5.21 26.0	62.5 -20.8		LIT CAN
71.5	17.	######################################		1.93	-57.5 -85.5	-219.H		-5.14	274768384488 2484784467	THE LIMI
4314	-7			1.93	-107.	-317.H	## 177			Ē
	10-L13	***********		1.50	-1.00K -1.00K	-2.00		-1.6 -1.6 -1.6 -1.6		
PARAMETER	ICC-SUPPLY CURRENT IEE-SUPPLY CURRENT		III FOR BITTE 5 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	FULL SCALE CURRTTL FULL SCALE CURRCHOS	ZERO SCALE CURRTTL ZERO SCALE CURRCMOS	102-DRIFT C BIPOLAR OFFSET CHRR.	1105) [C	-PSS1 (TTL) [+10%] -PSS1 (TTL) [-10%]		

TABLE 6.5. Device Type 01 Data at - 55°C.
MAN, FACTUMER CODE: 1 DEVICE TYPE: 568, TEMPERATURE: -56 DEG C , 25 CCT 79 1:116:30
PARAMETER

	255	1111111111111	555555 555555	GE ZZ	PPH/C	£ 33	33 555555555
	H	***********	44444444444444444444444444444444444444	2.56 2.50 1.00 1.00 1.00 1.00 1.00			A EFFEFFFFF
=	17.		######################################	1.99 1.99 -138.	-21.9M	4.0	
×	7.0			2.68 2.68 -124.	-176.M		
	10-Lin		**************************************	1.50 1.50 -1.00K	-2.00		44 EFFEFFFFF
PARAMETER	ICC-SUPPLY CURRENT IKE-SUPPLY CURRENT		IIL FOR WILL FOR WILL FOR WEILL FOR	FULL SCALE CURRTTL FULL SCALE CURRCMOS ZERO SCALE CURRTTL ZERO SCALE CURRCMOS	102-DRIFT	PSS2 (CNOS) [+ PSS2 (CNOS) [-	P6651

TABLE 6.5. Device Type 01 Data at - 55°C.

MANUTACTURER CODE: 1 DEVICE TYPE: 562; TEMPERATURE: -6E DEG C ; 26 OCT 79 11:16:5:0

PARANETER

	ro-rim	4310	4318	4313	+10+	4316		9	2	Ę			
SUM BIT ERROR(+) SUM BIT ERROR(-) SUM-ERROR(+)+ERROR(-)	222 222 227	185.3 -165.3 -40.83	24.0 24.9	-113.H	100.8 -816.8 -86.83	1.38.4 1.30.3	939.3 # - 47.64	14. 24. 25.	240.7 276.3 27.6.3	-301.n	2.50.2 2.50.2 2.50.2	# # # # # # # # # # # # # # # # # # #	223
GAIN ERROR (TTL) GAIN ERROR (CROS)	-25.0	-4.8 -5.81	-011.8	510.3 536.3	-8.80 -2.17	-614.7		14.3 1.3.3	 25	5.8 5.93		ZZ:	33
GAIN ERROR DRIFT (TTL)	-5.0	-494.N	465.M	1.71	1.31	200 . N		6.21	1.46	2.03		\$.	È
BIPOLAR OFFSET ERROR	-20.0	-1.35	-3.40	-1.25	-5.11	-3.98		-4.59	-1.56	-3.41		%	ş
POE DRIFT	-4.80	848.1	:	-326.M	-598.R	-346.M		:	-517.M	-134.R		:	È
+PSS1 (TTL) [+18%] +PSS1 (TTL) [-18%]	-866	-82.9	-118.	-99.0	-13S. -51.8	-119.		-133.	-51.7	-154.			33
MUR CARRY ERR-BITS 1	-986. -986.	96.1H	70.0M	51.1M	-286.M	121.R	*	469.H	535.8	766.R		8.5	151
MJR CARRY ERR-BITS 3	E. 005	-4.56H	-39.9H	-36.34	-274.1	-31.94	١	249.1	92.5H	263.H			55
FUR CARRY ERR-BILE 4	E . 000	76.67	-37.8M	134.1	162.1	55.34		132.4	31.23	13.78			121
MUR CARRY ERR-BITS 6	-900.₽	11.18	-10.43	14.93	-40.1M	12.8H		68.1M	-17.5M	13.7H		E. 996	158
HUR CARRY ERR-BITS 7	- 000	. 4.0 . 6.0 . .57	4.74 E.7.3	6.597	M. 94		38.45	46.07	-4.67N		E 1	18	
MJR CARRY ERR-BITS 9	E 000-	510.0	10.61	-53.60	46.04 FO.04	-16.6T		38.01 11.78	14.03 14.03 14.03				
MJR CARRY ERR-BITS 10	-900.H	17.54	16.9M	19.1M	23.6M	27.7M		443.0	5.76H	-16.9M		8	12
MJR CARRY ERR-BITS 11	-986.H	-18.6F	-14.6M	-27.8M	10.84	-8.50M		-18.48	-40.8H	-21.0M		E. 986	1.58

TABLE 6.5. Device Type 01 Data at -55°C.

***PRINTER CODE: | LEVICE TYPE: BGB; TEMPERATURE: -85 DEG C | 26 OCT '9 11:17:0: PARAMETER

LO-LIM

22	PPH/C	₽	PPR/C	33	
22 •••	8 .	20.0	*		
6.53	2. ea	-2.35	497.H	-131.	80881.4 80001.4 80001.6 8000000000000000000000000000000000000
#0 70 10	6.11	-1.63	295.R	-100. 57.3	6.00.00.00.00.00.00.00.00.00.00.00.00.00
**************************************	8 . 9	-80.0	8 .7		
gain error (TTL) gain error (CROS)	GAIN ERROR DRIFT (TTL)	BIPOLAR OFFSET ERROR	BPOE DRIFT	+PSS1 (TTL) [+10%] +PSS1 (TTL) [-10%]	MUR CARRY ERR-BITS 1 MUR CARRY ERR-BITS 2 MUR CARRY ERR-BITS 4 MUR CARRY ERR-BITS 6 MUR CARRY ERR-BITS 6 MUR CARRY ERR-BITS 7 MUR CARRY ERR-BITS 9 MUR CARRY ERR-BITS 9 MUR CARRY ERR-BITS 9 MUR CARRY ERR-BITS 9 MUR CARRY ERR-BITS 9 MUR CARRY ERR-BITS 11
	ERROR (171) -25.0 8.48 6.67 85.0 ERROR (CROS) -25.0 8.19 6.59 25.0	ERROR (CHOS) -25.0 8.48 6.67 85.0 ERROR (CHOS) -26.0 8.19 6.59 85.0 ERROR DRIFT (TTL) -5.00 6.11 2.02 5.00	ERROR (TTL) -25.0 8.48 6.67 25.0 ERROR DRIFT (TTL) -5.00 6.11 2.02 5.00 GANG OFFEE ERROR DRIFT (TTL) -5.00 6.11 2.02 5.00 GANG OFFEE ERROR -20.0 -1.63 -2.32 20.0	ERROR (TTL) -25.0 8.48 6.67 25.0 ENROR (CROS) -25.0 8.19 6.59 25.0 ERROR DRIFT (TTL) -5.00 6.11 2.02 5.00 LAR OFFSET ERROR -20.0 -1.63 -2.32 20.0 DRIFT -4.00 205.N 497.N 4.00	ERROR (TTL) -25.0 8.48 6.67 25.0 ENROR (CROS) -25.0 6.11 2.02 5.00 LAR OFFSET ERROR -20.0 -1.63 -2.32 50.0 DRIFT -4.00 295.N 497.N 4.00 LATL) E-1043 -200100131. 800. LTL) E-1043 -200100131. 800.

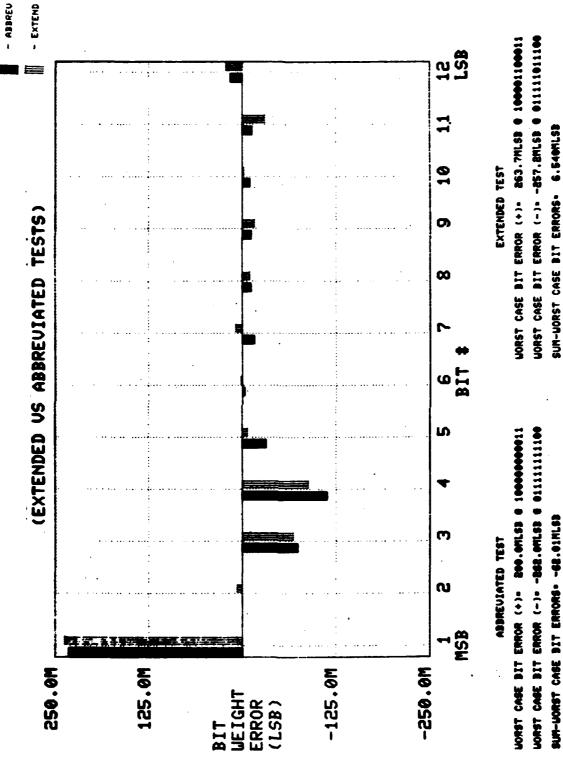
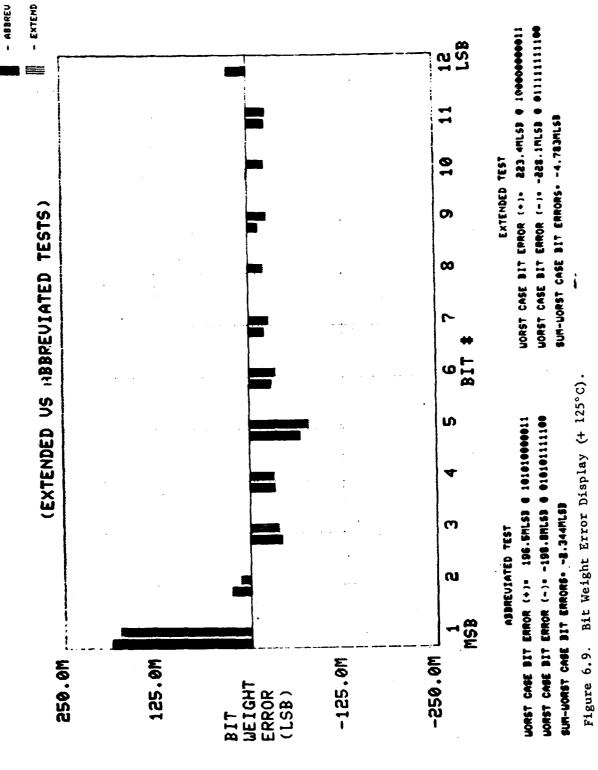


Figure 6.8. Bit Weight Error Display (+ 25°C).

VI-52



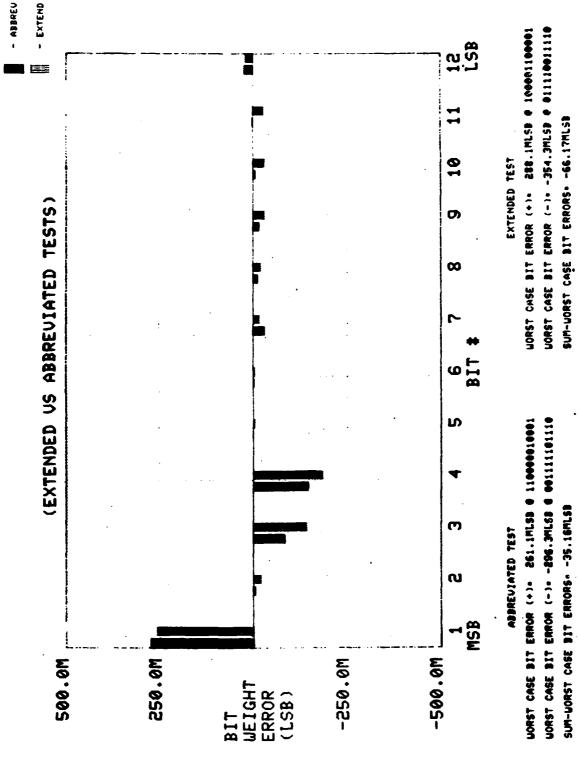


Figure 6.10. Bit Weight Error Display (- 55°C).

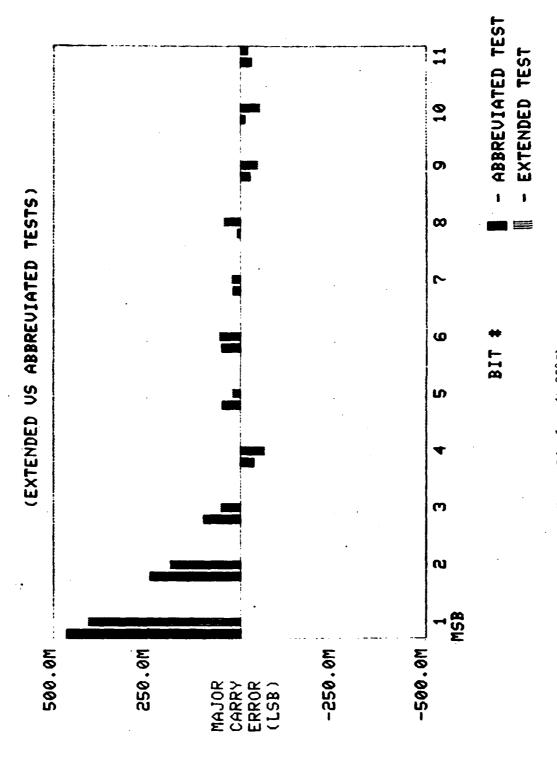


Figure 6.11. Major Carry Error Display (+ 25°C).

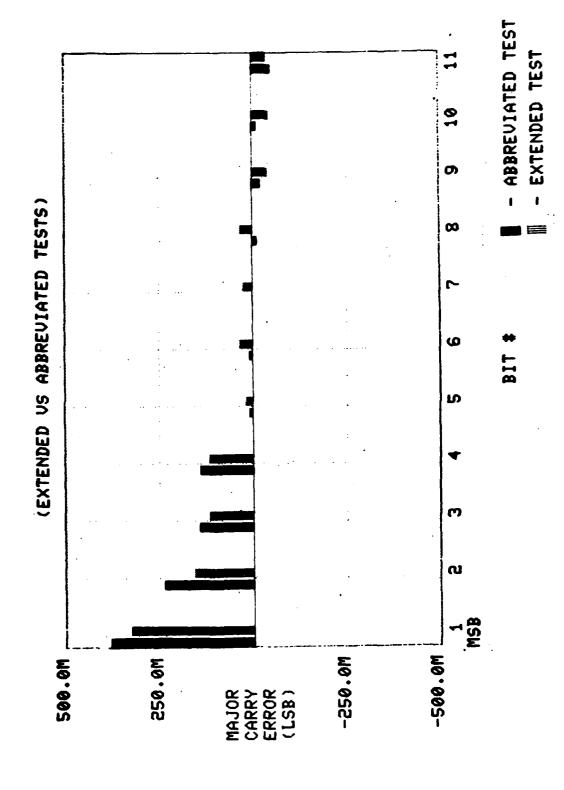


Figure 6.12. Major Carry Error Display (+ 125°C).

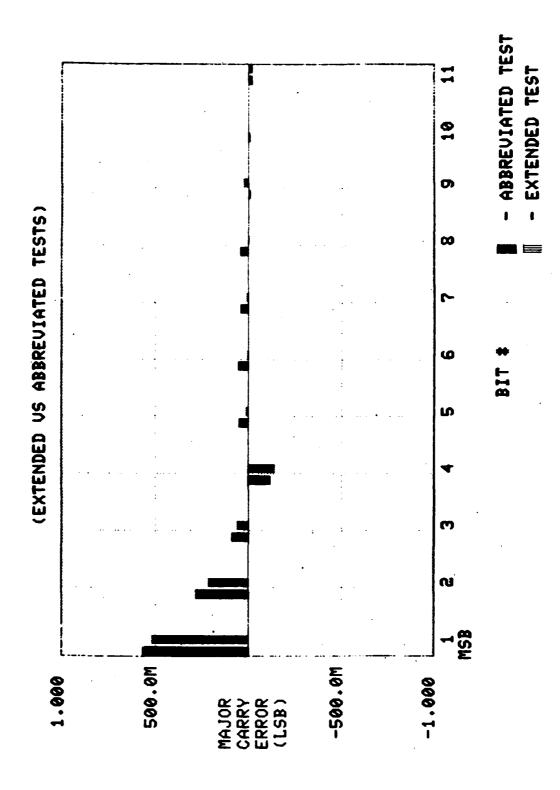
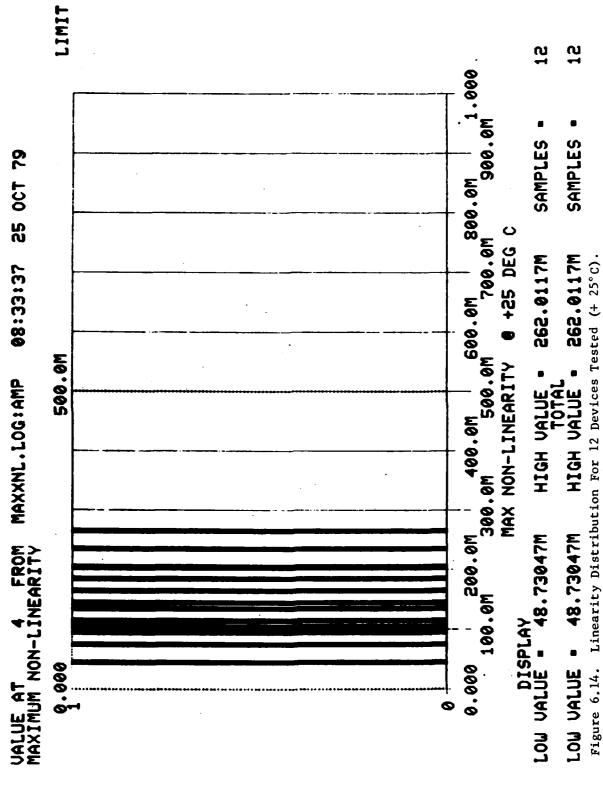
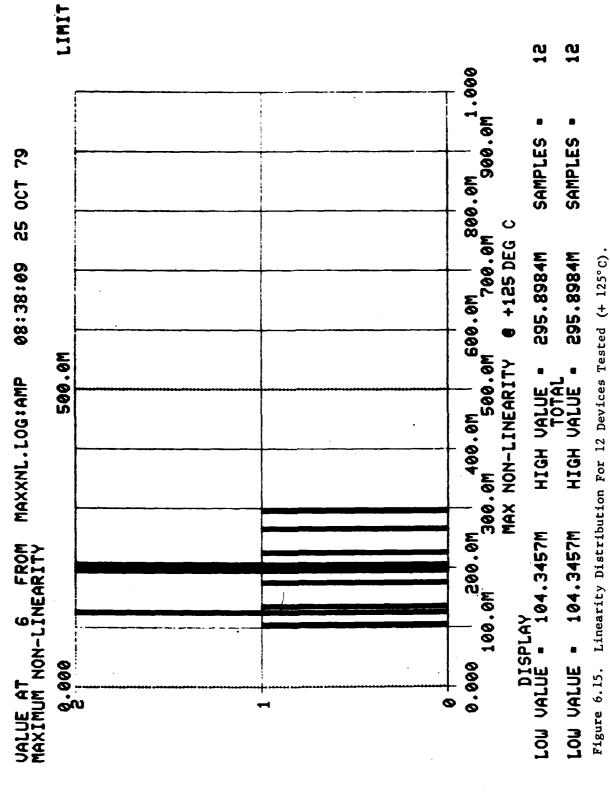


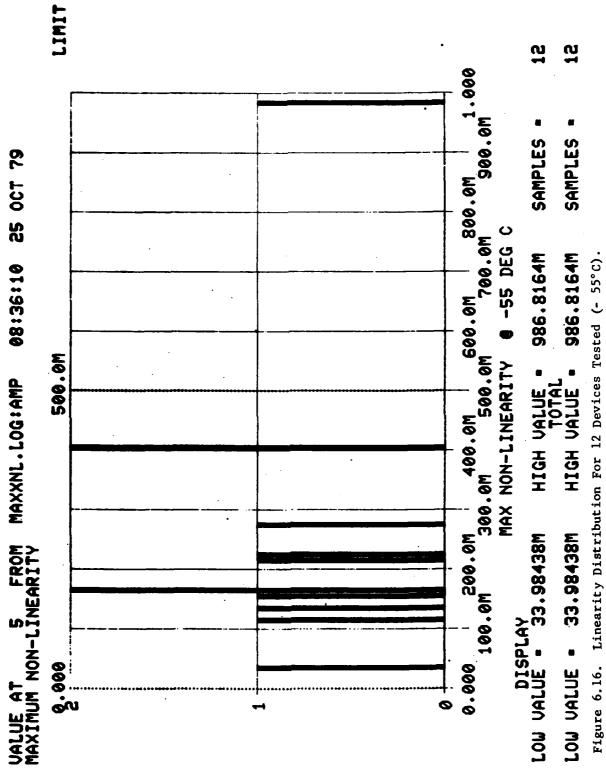
Figure 6.13. Major Carry Error Display (- 55°C).



VI-58



VI- 59



VI-60

SECTION VII

PRECISION VOLTAGE REFERENCES

MIL-M-38510/124

TABLE OF CONTENTS

		Page
	List of Figures	VII -ii
	List of Tables	VII -ii:
7.1	Introduction and Background	VII -1
7.2	Description of Devices	VII -1
7.3	Device Characterization	VII -3
7.4	Test Results and Evaluation of Data	VII -4
7.5	Conclusions and Recommendations	VII -6

LIST OF FIGURES

Figure	Title	Page
7.1	Subsurface Avalanche Zener Reference Diode	VII -1
7.2	Schematic of LM199A Voltage Reference	VII -2
7.3	Heater Power Dissipation versus Temperature for Different Reference Currents	VII -7
7.4	Reference Voltage and Noise Test Circuit	VII -8
7.5	Dynamic Impedance Test Circuit	VII -8
7.6	Population Histogram for LM129A Precision Voltage Reference	VII - 9
7.7	Population Histogram for LM199A Precision Voltage Reference	VII -10

LIST OF TABLES

Table	Title	Page
7.1	Summary of Measurements at $I_1 = 0.6$ mA (LM129A)	VII11
7.2	Summary of Measurements at $I_1 = 1.0$ mA (LM129A)	VII -12
7.3	Summary of Measurements at $I_1 = 15$ mA (LM129A)	VII -13
7.4	Summary of Measurements (LM129A)	VII -14
7.5	Summary of Measurements at $I_1 = 0$ mA; $V_s = 30$ V (LM199A)	VII -15
7.6	Summary of Measurements at $I_1 = 0.5$ mA; $V_S = 30$ V (LM199A)	VII -16
7.7	Summary of Measurements at $I_1 = 1.8 \text{ mA}$; $V_S = 30 \text{ V (LM199A)}$	VII -17
7.8	Summary of Measurements at $I_1 = 5$ mA; $V_S = 30$ V (LM199A)	VII -18
7.9	Summary of Measurements at $I_1 = 10 \text{ mA}$; $V_S = 30 \text{ V (LM199A)}$	VII -19
7.10	Summary of Measurements at $I_1 = 11.3 \text{ mA}$; $V_s = 30 \text{ V (LM199A)}$	VII -20
7.11	Summary of Measurements (LM199A)	VII -21
7.12	Summary of Measurements at $I_1 = 1.8 \text{ mA}$; $V_S = 9 \text{ V (LM199A)}$	VII -22
7.13	Summary of Measurements at $I_1 = 11.3 \text{ mA}$; $V_s = 9 \text{ V (LM199A)}$	VII -23
7.14	Summary of Measurements at $I_1 = 1.8 \text{ mA}$; $V_S = 40 \text{ V (LM199A)}$	VII -24
7.15	Summary of Measurements at $I_1 = 11.3 \text{ mA}$; $V_S = 40 \text{ V}$ (LM199A)	VII -25
7.16	Summary of Measurements at $I_1 = 1$ mA; $V_s = 30$ V (LM199A)	VII -26
7.17	Electrical Performance Characteristics for Device Types 01 & 02	VII -27

SECTION VII

CHARACTERIZATION OF PRECISION VOLTAGE REFERENCES

MIL-M-38510/124

7.1 Introduction and Background

As precision and accuracy of control systems increase, the need for a stable, precise voltage reference becomes apparent.

Precision voltage references are used in ratiometeric measurement system as a reference against which all signal voltages can be compared, and especially for high accuracy data converters.

The two precision voltage references characterized for this slash sheet are the LM129A and the LM199A. These devices were selected by RADC, GEOS and members of the JC-41 Committee for characterization. The

LM129A's and LM199A's were tested in test circuits devised to check each parameter at all of the specified temperatures.

7.2 Description of Device Types ·

The LM129A and LM199A precision voltage references each incorporate precision temperature compensated 6.9 volt zener references. The design of the silicon chips uses a subsurface zener diode reference to reduce noise and long term stability. This construction shown in Figure 7.1, is accomplished using a relatively new technique known as ion implantation. The subsurface diode is buried below the chip surface and is therefore shielded from surface contamination and from ion inversion and noise problems common to regular zener breakdown diodes.

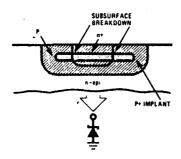


Figure 7.1. Subsurface Avalanche Zener Reference Diode

The voltage reference, additionally, contains circuitry to buffer the temperature compensated zener diode from current variations that accompany load current changes. The circuit for the LM199A precision voltage reference is shown in Figure 7.2.

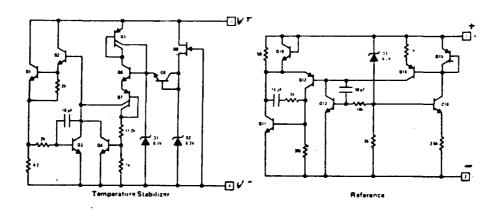


Figure 7.2. Schematic of LM199A Voltage Reference.

The precision reference circuit in this figure is comprised of two circuits on a single monolithic silicon chip. One circuit is a temperature stabilizer. The other circuit is the voltage reference. The voltage reference consists of a reference diode, D3, a current shunt circuit, Q10-Q13 and a current mirror, Q14-Q16. The reference diode is temperature compensated by adjusting the diode current for O-T.C. This is accomplished by adjusting the 10K A resistor in the base of transistor Q13. Transistor Q13 serves to buffer any reference circuit current variations from the reference diode. For example, if the external load current suddenly decreases, the current through the external series resistance from the main supply will tend to decrease, and the voltage across the reference will tend to increase. The increased voltage across the reference will cause more current to flow in the base of transistor Q13. Since transistor Q13 supplies base current for the current shunt, the current shunt also conducts more current. By adjusting the 30 K. resistor in the collector of Q12, the increase in shunt current can be made approximately equal to the decrease in current supplied to the load. The only current change to the reference diode is due to the small change in transistor Q13 base current. Transistors 014-016

form a current mirror and serve as a constant current, active load for transistor Q13. Because the reference diode is temperature compensated and because the current shunt handles the main variations in current, the reference circuit maintains a stable output voltage for large variations of both temperature and current. This stability is observed in both the LM1.9A and LM1.99A precision references.

The LM199A differs from the LM129A in that it also contains a temperature stabilizer circuit. The temperature stabilizer circuit operates from a separate supply voltage that can range from 9V to 40 V. The circuit draws current from this supply so as to maintain a constant chip temperature of approximately 85°C. As the chip ambient temperature decreases, the stabilizer draws more current from the supply and increases the power dissipation on the chip. Thus, the chip temperature tends to remain constant. A plot of average power dissipation versus temperature and supply voltage is shown in Figure 7.3. A thermal insulator housing is used with the LM199A to aid in the maintenance of a constant chip temperature. For temperatures above 85°C, the temperature stabilizer is no longer effective and the LM199A precision reference performance is essentially degraded to that of the LM129A.

7.3 Device Characterization

All evaluation and characterization of the precision voltage references was performed in bench test set-ups, and measurements were made on an HP3455 using Kelvin connections to the DUT. Breakdown voltage measurements were made at different current levels and at different temperatures, -55° C, 25° C, $(85^{\circ}$ C) and 125° C. Noise, Dynamic Impedance and Warm-up were performed at one current level at 25° C.

Figure 7.4 shows the test circuit used to measure breakdown voltage. The breakdown voltage measurements on the LM129A devices were made at current levels of 0.6 mA; 1.0 mA and 15 mA. For the LM199A, these measurements were made at current levels of 0.5 mA, 1.8 mA, 5 mA, 10.0 mA and 11.3 mA with the temperature stabilizer supply voltages set at 30 volts. Additional measurements were made with the temperature stabilizer supply voltages set at 9 volts and 40 volts.

The noise test circuit is shown in Figure 7.4. Measurements were made on a Tektronix model 7904 oscilloscope with a model 7A22 differential input preamplifier. The bandwidth on the preamp was adjusted for $10~{\rm Hz} \le {\rm BW} \le 10~{\rm kHz}$ and peak-to-peak measurements were made on the oscilloscope.

The dynamic impedance test circuit is shown in Figure 7.5. Measurements were made using a 400 Hz signal source and a voltmeter with a 400 Hz narrow band filter. AC signal levels were low in order to insure small signal impedance measurements. Kelvin connections were used and contact was made 1/8" below the reference case.

The initial temperature stabilizer supply current was measured using a Tektronix model storage oscilloscope with a current probe. The peak current was recorded from the oscilloscope.

7.4 Test Results and Evaluation of Data

The data taken on these devices was analyzed to determine the average value and standard deviation. The results of this analysis are shown in Tables 7.1 through 7.15.

The tables show two columns for average value and two columns for standard deviation. The two columns to the extreme right of each table indicate the final average value and the final standard deviation value after the non-typical data is removed from the analysis. The other two columns for average value and standard deviation value are computed from all of the data measurements.

The data was obtained from 21 parts and 13 parts for the LM129A and the LM199A. Statistical analysis on these devices is inconclusive because of the small sample size, however, the characterization failed to uncover any major devices anomalies, and some of the measurements were out of the specified tolerance. Some of the data taken was strictly for characterization and provides data on conditions not specified by the vendor or recommended for the device slash sheet.

Tables 7.1 through 7.4 tabulate the analyzed, measured data taken on the LM129A. Measurements were made on the devices with supply currents of .6 mA, 1.0 mA and 15 mA. The reference voltage measurements were all well within the manufacturer's specified limits and a population hystogram of these voltages is shown in Figure 7.6. The devices all had measured output voltages slightly below the nominal of 6.95 \pm .25 volts. The mean value for I_1 = 1 mA was 6.8724 with a standard devication of .02 volts.

Data for the evaluation of temperature coefficient was obtained by measuring the output voltage at the various specified temperatures and determining the measurement differences in PPM/°C. The mean temperature coefficient for this current was - 0.3 PPM/°C with a standard deviation

of 3.1 PPM/°C for a temperature range from - 55°C to 25°C. The mean temperature coefficient over the temperature range from 25°C to 125°C was + 3.8 PPM/°C with a standard deviation of 2.8 PPM/°C. These numbers are well within the specification of ± 10 PPM/°C. For this characterization effort similar data was obtained for device currents of .5 mA and 15 mA. This data was used in the analysis of temperature coefficien change with current. The analysis shows that the data for T.C. change with current, over the temperature range from 25°C to 125°C, is greater than the vendor's "typical" specification. The mean value was determined as - 1.9 PPM/°C and the standard deviation was 1.3 PPM/°C, however, the parts received by OS were not screened for this parameter.

Tables 7.5 through 7.15 tabulate the analysis of the measured data for the LM199A. Data was taken to determine the power dissipation of the thermal stabilizer versus temperature. The results of this data are tabulated in Table 7.5 and are graphed on Figure 7.3. The graph shows the linearity of the change in power dissipation versus temperature for zero current in the reference voltage circuit. From this information the average thermal resistance is calculated as

$$\theta = \frac{538.7 - 78.0}{85 + 55} = 3.29 \text{ mW/°C}$$

The vendor was contacted on this matter and confirmed that the figure should be 2 - 5 mV/°C. The vendor recommends that the thermal resistance should be nominally specified at 5 mW/°C. The total device power dissipation is the sum of the thermal stabilizer circuit power and the reference voltage circuit power. ($P_T = P_{TS} + P_R$). The graph in Figure 7.3 shows how the thermal stabilizer power dissipation is affected by the added power dissipation of the voltage reference.

Data taken for various reference voltage currents was taken with the thermal stabilizer supply voltage set to 30 volts. The reference voltage current values varied from .5 mA to 11.3 mA. Since the thermal stabilizer temperature is not regulated to the maximum temperature of 125°C, two temperature coefficient specifications are required. One T.C. tolerance of .5 PPM/°C covers the temperature range from -55°C to 85°C. The other tolerance of 10 PPM/°C covers the temperature range from 85°C to 125°C. Data presented in Tables 7.6 to 7.10 shows that T.C. range increases as the current through the reference voltage circuit increases. For currents of 5 mA and larger, the standard deviatio of the temperature coefficients is larger than the 1 mA limit for a temperature range from 25°C to 85°C, however, these devices will be tested only at $I_1 = 1$ mA. The vendor was contacted and stated that thi and other parameters can be screened for special applications.

Table 7.11 tabulates the results of the analyzed data for dynamic impedance, noise and T.C. changes with current. Noise measurements were made by determining the peak-to-peak value of the noise. The mean value of these measurements was 73.5 uV p-p. For broad-band white noise, (RMS value)= (peak-to-peak value)/6. Therefore, the mean RMS value is 12.25 uV, which is less than the manufacturer's specification. As previously described, the temperature coefficient increases with reference voltage current. The affects of this anomally on temperature coefficient change with current are shown in Table 7.11. The most significant tolerance variation occurs for a temperature range of 25°C to 85°C where the standard deviation is 1.3 PPM/°C.

Tables 7.12 through 7.15 provide additional data on the measurement of reference voltage, temperature coefficient and thermal stabilizer power dissipation. For these measurements the reference voltage current was set to 1.8 mA and 11.8 mA and the thermal stabilizer voltage was set to 9 volts and 40 volts. The data results were consistent with previous measurements and no anomalies were observed.

Table 7.16 tabulates the analysis of measured data for LM199A Thermal Stabilizer Initial current, Reference Voltage Warm-up Stability and Reference Voltage Temperature Cycling Hysteresis.

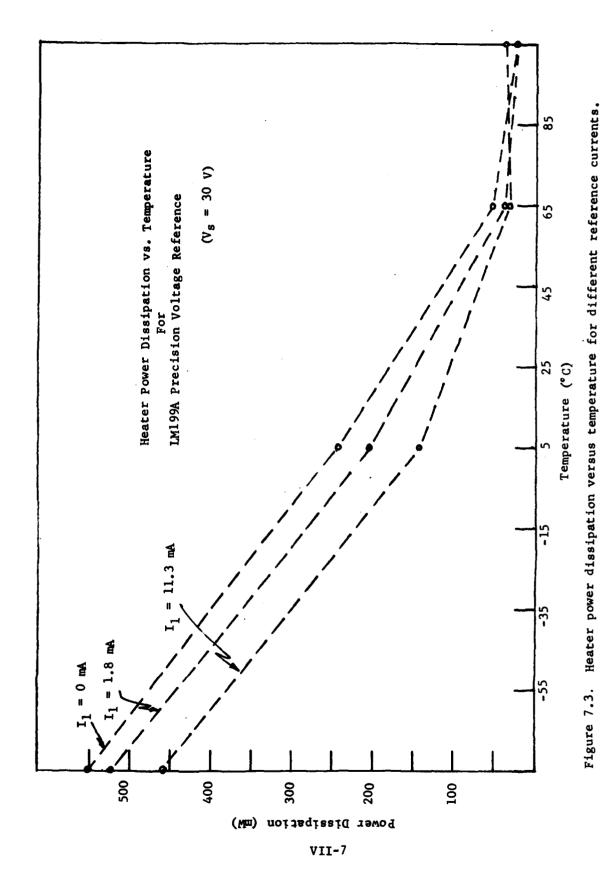
7.5 Conclusions and Recommendations

The data obtained for these analyses showed that the reference voltage devices met the specifications published by the manufacturer. Other parameters, not one hundred percent guaranteed by the manufacturer but recommended by the JC-41 Committee, were measured and the data was analyzed. Data taken on the temperature coefficient change with current showed that some devices had values much greater than the published typical value. The manufacturer states that this parameter can be guaranteed but the additional tests will add extra cost to the parts. It was decided not to recommend specification of this parameter.

Additional tests, such as, power off/on repeatibility, warm-up stability, and temperature cycling hysteresis have been checked. These parameters require extreme care in order to obtain reliable test data. The power off/on data was obtained as a consequence of the warm-up test data at time = 5 min. These data are shown in Table 7-16. OS does not recommend that the power off/on and warm-up test be a part of the slash sheet.

No major anomalies were uncovered during this characterization. A minor anomaly was observed in the measurement of temperature coefficient change with current. As the voltage reference current and temperature were increased simultaneously to their maximum, the T.C. change increased until it was 2-3 times the value at low current and temperature.

Table 7.17 lists the recommended parameters for these devices.



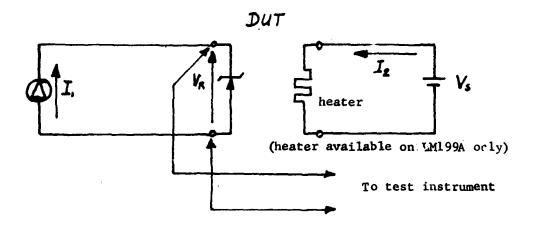


Figure 7.4. Reference voltage and noise test circuit.

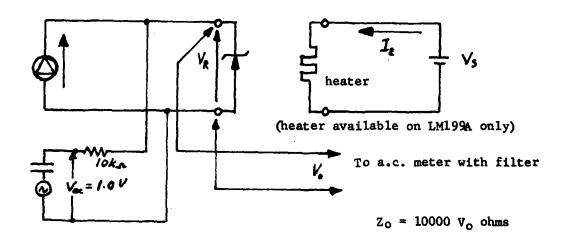


Figure 7.5. Dynamic impedance test circuit.

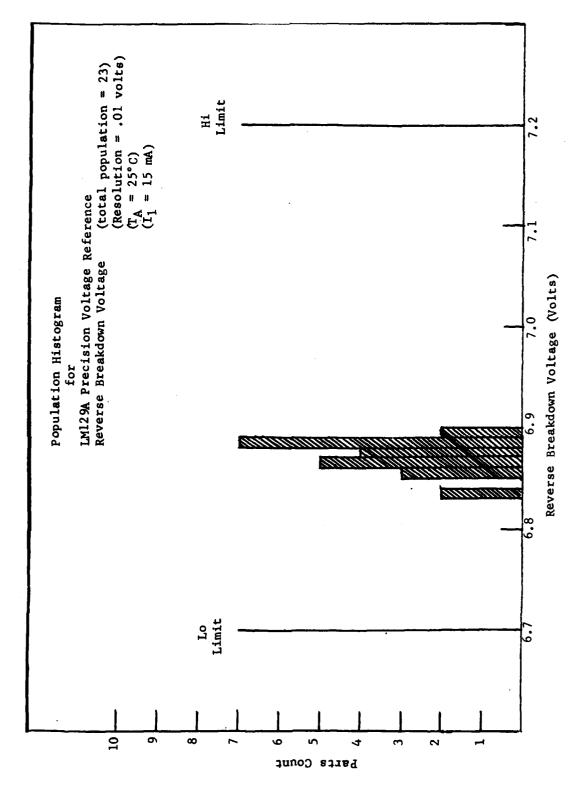


Figure 7.6. Population histogram for LM129A precision voltage reference.

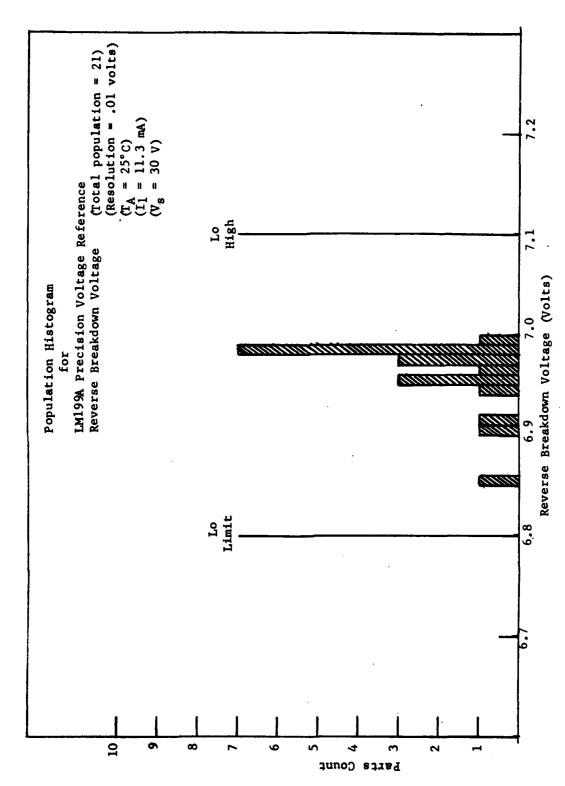


Figure 7.7. Portuation histogram for LM199A precision voltage reference.

Table 7.1. Summary of Measurements at $I_1 = 0.6 \text{ mA}^{\frac{1}{2}}$ (LM129A)

Parameter	2/ Overall Average	Overall	Parameter values not included in Final Average and Final 7, and associated devices	1 ~ /	Final
Reference Voltage at 25°C (volts)	High = +6.8922 +6.8718 Low = +6.8360	.02	None Manufacturer's spec = 6.95 ± .25 V	High = +6.8922 +6.8718 Low = +6.8360	.02
T _c over range -55°C € T _A €25° (PPM/°C)	High = +4.2 C -0.5 Low = -6.1	3.0	None Manufacturer's spec = ± 10 PPM/°C	High = +4.2 -0.5 Low = -6.1	3.0
T _c over range 25°C ≼ T _A ≼ 25° (PPM/°C)	High = +8.0 C + 3.8 Low = -7.7	3.6	None Manufacturer's spec = ±10PPM/°C	High = +8.0 +3.8 Low = -7.7	3.6

Notes: 1. $I_1 = current through voltage reference.$

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.2. Summary of Measurements at $I_1 = 1 \text{ mA}^{\frac{1}{2}}$ (LM129A)

Parameter	2/ Overall Voltage	Overall	Parameter values not included in Final Average and Final σ , and associated device $\#$		Final
Reference Voltage at 25°C (volts)	High = +6.8927 +6.8724 Low = +6.8365	.02	None Manufacturer's spec = 6.95 ± .25V	High = +6.8927 +6.8724 Low = +6.8365	.02
T _c over range -55°C≰T _A ≰25° (PPM/°C)		3.1	None Manufacturer's spec = ± 10 PPM/°C	High = +4.2 -0.3 Low = -6.8	3.1
T _c over range 25°C ← T _A ← 125		2.8	None Manufacturer's spec = ± 10 PPM/°C	High = +7.2 +3.8 Low = -2.5	2.8

Notes: 1. I_1 = current through voltage reference.

^{2.} Each block in the average column indicates the high value, the computed average value and the low value for the specified parameter.

Table 7.3. Summary of Measurements at $I_1 = 15 \text{ mA}^{\frac{1}{2}}$ (LM129A)

Parameter	2/ Overall Average	Overall	Parameter values not included in Final Average and Final \mathcal{T} , and associated device $\#$		Final
Reference Voltage at 25°C (volts)	High = +6.9036 +6.8852 Low = +6.8455	.02	None Manufacturer's spec = 6.95 ± .25V	High = +6.9036 +6.8852 Low = +6.8455	.02
T _c over range -55°C ≤ T _A ≤ 25 (PPM/°C)	High = +2.3 °C -1.8 Low = -7.3	2.8	None Manufacturer's spec = ± 10 PPM/°C	High = +2.3 -1.8 Low = -7.3	2.8
T _C over range 25°C ≤ T _A ≤ 125 (PPM/°C)		2.7	None Manufacturer's spec = ± 10 PPM/°C	High = +8.4 +4.5 Low = -1.2	2.7

Notes: 1. $I_1 = current through voltage reference.$

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.4. Summary of Measurements

(LM129A)

Parameter	2/ Overall Average	Overall	Parameter values not included in Final Average and Final σ , and associated device $\#$	ı — ·	Final
P-P Noise (uV)	69.8	4.9	None Manufacturer's spec = 20 (RMS max)	69.8	4.9
Change in reverse break-down temperature coefficient with current 1 mA \leq I ₁ \leq 15 mA ¹ /-55° C \leq T _A \leq 25° C	High = +2.1 +0.8 Low = -1.2	0.8	None Manufacturer's spec = ± 1 PPM/°C (Typus)	High = +2.1 +0.8 Low = -1.2	0.8
Change in re- verse break- down tempera- ture coefficient 1 mA ≤ I ₁ ≤ 15 mA 1/ 25°C ≤ T _A ≤ 125°C	High = +0.6 -1.9 Low = -5.2	1.3	None Manufacturer's spec = ± 1 PPM/°C (Typecel)	High = +0.6 -1.9 Low = -5.2	1.3
Dynamic Impedance (ohms)	.74	.24	None Manufacturer's spec = 1	.74	.24

Notes: 1. I₁ = current through voltage reference.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.5. Summary of Measurements at $I_1 = 0$ mA; $V_s = 30 \text{ V}^{\frac{1}{2}}$ (LM199A)

	<u>2</u> / Overall	Overall	Parameter values not included in Final Average and Final T,		Final
Parameter	Average	_6~	and associated device #	Average	5
Reference Voltage at 25°C (volts)	•	-	-	_	<u>-</u>
T _c over range -55°C ∉T ∉ 25°C (PPM/ [⊕] C)	-	-	-	-	-
T over range 25°C ≰T _A ≰ 85°C (PPM/°C)	-	-	<u>-</u>	-	-
T over range 85°C ≰T _A ≰ 125°C (PPM/°C)	-	_	-	-	- .
Heater Power dissipation at TA = -55°C (mW)	High = 578.3 538.7 Low = 512.4	21.1	None	High = 579.3 538.7 Low = 512.4	21.1
Heater Power dissipation at TA = 25°C (mW)	High = 252.6 229.4 Low = 213.3	13.0	None	High = 252.6 229.4 Low = 213.3	13.0
Heater Power dissipation at TA = 85°C (mW)	High = 78.0 52.8 Low = 28.5	18.1	None	High = 78.0 52.8 Low = 28.5	18.1
Heater Power dissipation at T _A = 125°C (mW)	High = 25.5 22.7 Low = 20.2	1.7	None	High = 25.5 22.7 Low = 20.2	1.7

Notes: 1. I_1 = current through voltage reference. v_s = temperature stabilizer voltage.

^{2.} Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.6. Summary of Measurements at $I_1 = .5 \text{ mA}$; $v_s = 30 \text{ v}^{\frac{1}{2}}$ (LM199A)

Parameter	2/ Overall Average	Overall	Parameter values not included in Final Average and Final T, and associated device #		Final
Reference Voltage at 25°C (volts)	High = +6.9899 +6.9582 Low = +6.9025	.03	None Manufacturer's spec = +6.95 ± .15	High = +6.9899 +6.9582 Low = +6.9025	.03
T _c over range -55°C ≤ T _A ≤ 25°C (PPM/°C)	High = 0.031 Low =54	.17	None Manufacturer's spec = .5	High = 0.031 Low =54	.17
T _C over range 25°C ≤ T _A ≤ 85°C (PPM/°C)	High = + .2450 Low =95	.34	None Manufacturer's spec = .5	High = +.24 50 Low = 95	. 34
T _C over range 85°C ₹ T _A ₹ 125°C (PPM/°C)	High = +7.5 +1.7 Low = -9.4	5.0	None Manufacturer ⁹ s spec = 10	High = +7.5 +1.7 Low = -9.4	5.0

Notes: 1. I_1 = current through voltage reference V_s = temperature stabilizer voltage 2. Each block in the average column includes the high value, the

Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.7. Summary of Measurements at $I_1 = 1.8 \text{ mA}$; $V_s = 30 \text{ V}^{\frac{1}{2}}$ (LM199A)

	<u>2</u> /		Parameter values not included	2/	
	Overall	1	in Final Average and Final ${\mathcal T}$,		Final
Parameter	Average	6	and associated device #	Average	0
Reference Voltage at 25°C (volts)	High = +6.99376 +6.95932 Low = +6.84427	.03	None Manufacturer's spec = 6.95 ± .15 V	High = +6.99376 +6.95932 Low = +6.84427	.03
T _C over range -55°C ←T _A ← 25°C (PPM/°C)	High = +.72 -0.4 Low = -10.0	2.4	-3.2, device #12 -10.0, device #15 Manufacturer's spec = .5	High = +.72 +0.3 Low = 0.0	0.2
T _C over range 25°C ←T _A ← 85°C (PPM/°C)	High = +0.7 +.32 Low = 0.0	0.3	None Manufacturer's spec = 5	High = +0.7 +.32 Low = 0.0	0.3
T _C over range 85°C∉T _A ←125°C (PPM/°C)	High = +9.3 +0.6 Low = -11.3	6.6	None Manufacturer's spec = 1 0	High = +9.3 +0.6 Low = -11.3	6.6
Heater Power dissipation at T _A = -55°C (mW)	High = 567.0 522.0 Low = 491.7	22.3	None	High = 567.0 522.0 Low = 491.7	22.3
Heater Power dissipation at T _A = 25°C (mW)	High = 240.9 213.6 Low = 192.0	14.8	None	High = 240.9 213.6 Low = 192.0	14.8
Heater Power dissipation at T _A = 85°C (mW)	High = 65.7 41.3 Low = 20.7	18.0	None	High = 65.7 41.3 Low = 20.7	18.0
Heater Power dissipation at TA = 125°C (mW)	High = 25.2 22.5 Low = 20.0	1.7	None	High = 25.2 22.5 Low = 20.0	1.7

Notes: 1. I_1 = current through voltage reference. V_s = temperature stabilizer voltage.

^{2.} Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.8. Summary of Measurements at $I_1 = 5$ ma; $V_s = 30$ $V_s^{1/2}$ (LM199A)

Parameter	2/ Overall Average	Overall	Parameter values not included in Final Average and Final T, and associated device #		Final
Reference Voltage at 25°C (volts)	High = +6.9929 +6.9613 Low = +6.9055	.03	None Manufacturer's spec =	High = +6.9929 +6.9613 Low = +6.9055	.03
T _C over range -55°C≤T _A ≤25°C (PPM/°C)	High = +.54 .03 Low =54	.25	None Manufacturer's spec = .5	High = +.54 .03 Low = 54	.25
T over range 25°C≤T ≤ 85°C (PPM/°C)	High = +1.9 +.28 Low =72	.80	None Manufacturer's spec = .5	High = +1.9 +.28 Low =72	.80
T _C = over range 85°C & T _A & 125°C (PPM/°C)	High = +9.7 +3.0 Low = -8.7	5.5	None Manufacturer's spec = 10	High = +9.7 +3.0 Low = -8.7	5.5

Notes: 1. I_1 = current through voltage reference V_8 = temperature stabilizer voltage

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.9. Summary of Measurements at $I_1 = 10 \text{ mA}$; $V_s = 30 \text{ N}^{-1}$ (LM199A)

Parameter	2/ Overall Average	Overall	Parameter values not included in Final Average and Final σ , and associated device #	,	Final
Reference Voltage at 25°C (volts)	High = +6.9955 +6.9640 Low = +6.9085	.03	None Manufacturer's spec = +6.95 ± .15	High = +6.9955 +6.9640 Low = +6.9085	.03
T over range -55°C≤TA≤ 25°C (PPM/°C)	High = +.72 +.36 Low =18	.23	None Manufacturer's spec = .5	High = +.72 +.36 Low = 18	.23
T _C over range 25°C ≤ T _A ≤ 85°C (PPM/°C)	High = +1.9 +.91 Low = -1.2	. 90	None Manufacturer's spec = .5	High = +1.9 +.91 Low = -1.2	. 90
T over range 85°C≰T _A ≰ 125°C (PPM/°C)	High = +10.0 +2.8 Low = -10.5	6.4	None Manufacturer's spec = 10	High = +10.0 +2.8 Low = -10.5	6.4

Notes: 1. I_1 = current through voltage reference V_s = temperature stabilizer voltage 2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.10. Summary of Measurements at $I_1 = 11.3 \text{ mA}$; $V_s = 30 \text{ V}^{1/2}$ (LM199A)

Parameter	2/ Overall (Average	overall	Parameter values not included in Final Average and Final σ , and associated device #	2/ Final Average	Final
Reference Voltage at 25°C (volts)	High = +6.99934 +6.96484 Low = +6.85108	0.3	None Manufacturer's spec = 6.95 ± .15 V	High = +6.99934 +6.96484 Low = +6.85108	.03
T _C over range -55°C ≤ T _A ≤ 25°C (PPM/°C)	High = +9.5 +0.9 Low = -4.3	2.4	-4.3, device #12 +9.5, device #13	High = +1.6 +0.7 Low = 36	0.4
T _C over range 25°C ≼T _A ≰85°C (PPM/°C)	High = +4.8 +2.5 Low = -0.7	1.5	+4.8, device #5 +3.6, device #17	High = +3.3 +2.2 Low = -0.7	1.4
T _C over range 85°C ≤T _A ≤ 125°C (PPM/°C)	High = +7.3 -1.0 Low = -15.7	5.5	-15.7 device #1	High = +7.3 +.05 Low = -7.6	4.1
Heater Power dissipation at TA = -55°C (mW)	High = 501.9 458.4 Low = 425.7	24.2	None	High = 501.9 458.4 Low = 425.7	24.4
Heater Power dissipation at TA = 25°C (mW)	High = 174.6 146.8 Low = 121.8	14.9	None	High = 174.6 146.8 Low = 121.8	14.9
Heater Power dissipation at T _A = 85°C	High = 42.9 32.8 Low = 23.4	6.2	None	High = 42.9 32.8 Low = 23.4	6.2
Heater Power dissipation at TA = 125°C (mW)	High = 51.1 41.7 Low = 32.3	6.1	None	High = 51.1 41.7 Low = 32.3	6.1

Notes: 1. I_1 = current through voltage reference. V_s = temperature stabilizer voltage.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

VII -20

Table 7.11. Summary of Measurements (LM199A)

Parameter Dynamic Impedance (ohms)	1/ Overall Average High = .83 .66 Low = .3	Overall	Parameter values not included in Final Average and Final \mathcal{T} , and associated device $\#$ None Manufacturer's spec = 1 (max)	1/ Final Average High = .83 .66 Low = .3	Final 0
Peak to Peak Noise (uV)	High = 80 73.5 Low = 50	6.9	None Manufacturer's spec = 20 (RMS max)	High = 80 73.5 Low = 50	6.9
•	+10.7 +1.4 Low =	3.1	+9.1, device #14 +10.7, device #16	High = +1.1 +0.3 Low = -1.1	0.5
Change in reverse breakdown temp-erature coefficient with current 1.8mA ≤ I₁ ≤ 11.3mA 25°C ≤ TA ≤ 85°C	+4.8 +2.2 Low =	1.4	+4.8, device #17	High = +3.6 +2.0 Low = -0.7	1.3
	+8.6 -1.7 Low =	3.4	None	High = +8.6 -1.7 Low = -4.5	3.4

Note: 1. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.12. Summary of Measurements at $I_1 = 1.8 \text{ mA} \div V_s = 9 \text{ V}^{\frac{1}{2}}$ (LM199A)

Parameter	2/ Overall Average	Overall	Firameter values not included n Final Average and Final σ , and associated device #		Final
Reference Voltage at 25°C (volts)	High = +6.99343 +6.95897 Low = +6.84392	•03	None Manufacturer's spec = 6.95 ± .15 V	High = +6.93343 +6.95897 Low = +6.84392	.03
T _C over range -55°C≤T _A ≤ 25°C (PPM/°C)	High = +1.6 +0.2 Low = -16.3	3.9	-16.3, device #15	High = +1.6 +1.2 Low = +.72	0.3
T _c over range 25°C≤T _A ≤85°C (PPM/°C)	High = +1.4 +1.1 Low = +0.5	0.3	None	High = +1.4 +1.1 Low = +0.5	0.3
T _C over range 85°C € T _A € 125°C (PPM/°C)	High = +10.0 -3.0 Low = -63.0	17.1	-19.0, device #1 -63.0, device #19	High = +10.0 +2.4 Low = -9.4	5.6
Heater Power dissipation at TA = -55°C (mW)	High = 569.7 521.6 Low = 476.1	27.1	None	High = 569.7 521.6 Low = 476.1	27.1
Heater Power dissipation at TA = 25°C (mW)	High = 243.0 214.6 Low = 190.8	15.2	None	High = 243.0 214.6 Low = 190.8	15.2
Heater Power dissipation at TA = 85°C (mW)	High = 67.2 41.6 Low = 14.4	19.1	None	High = 67.2 41.6 Low = 14.4	19.1
Heater Power dissipation at TA = 125°C (mW)	High = 7.2 6.4 Low = 5.5	0.6	None	High = 7.2 6.4 Low = 5.5	0.6

Notes: 1. I_1 = current through voltage reference. V_s = temperature stabilizer voltage.

^{2.} Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.13. Summary of Measurements at $I_1 = 11.3 \text{ mA}$; $V_s = 9 \text{ V}^{1/2}$ (LM199A)

			,		
•	2/		Parameter values not included		
.	Overall	1	in Final Average and Final σ ,	I .	Final
Parameter	Average.	~	and associated device #	Average	~
Reference	High =	ļ		High =	1
Voltage at	+6.99912		<u> </u> -	+6.99912	1
25°C (volts)	+6.96457	.03	None	+6.96457	.03
	Low =		Manufacturer's spec =	Low =	l
	+6.85086		6.95 ± .15 V	+6.85086	
T _c over range	High =			High =	İ
-55°C ≤T A ≤ 25°C	+1.8			+1.8	
(PPM/°C)	+1.5	0.3	None	+1.5	0.3
	Low =		 :	Low =	
	+.54			+.54	
T _c over range	High =		+4.1, device #5	High =	}
25°C ← T _A ≤ 85°C	+5.5		+5.5, device #17	+3.4	
(PPM)°C)	+2.6	1.3		+2.3	1.0
	Low =			Low =	
	+.5			+.5	L
T _c over range	High =		-28.5, device #1	High =	
85°C ≼ T _A ≤ 125°C	+148.7		+148.7, device #16	+11.4	
(PPM/°C)	+8.8	38.6	"	+0.9	7.2
•	Low =			Low =	
	-28.5		<u> </u>	-13.7	
Heater Power	High =			High =	
dissipation at	504.0	ĺ		504.0	
$T_{\Delta} = -55^{\circ} \text{C (mW)}$	457.6	24.5	None	457.6	24.5
A	Low =			Low =	İ
	421.2			421.2	İ
Heater Power	High =			High =	
dissipation at	179.8			179.8	
$T_A = 25^{\circ}C \text{ (mW)}$	150.4	15.7	None	150.4	15.7
	Low =	•		Low =	1
	124.6		· · · · · · · · · · · · · · · · · · ·	124.6	
Heater Power	High =			High =	
dissipation at	12.1			12.1	
$T_A = 85^{\circ}C \text{ (mW)}$	9.0	1.8	None	9.0	1.8
Α , ,	Low =			Low =	1
	6.9			6.9	
Heater Power	High =			High =	
dissipation at	14.2			14.2	
$T_A = 125^{\circ}C \text{ (mW)}$	11.5	1.8	None	11.5	1.8
- A	Low =			Low =]
	8.8	}	·	8.8	
			 		

Notes: 1. I_1 = current through voltage reference. V_s = temperature stabilizer voltage.

 Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

VII -23

Table 7.14. Summary of Measurements at $I_1 = 1.8 \text{ mA}$; $V_s = 40 \text{ V}^{\frac{1}{2}}$ (LM199A)

Parameter	2/ Overall Average	overall	Parameter values not included in Final Average and Final σ , add associated device $\#$		Final
Reference Voltage at 25°C (volts)	High = +6.99383 +6.95949 Low = +6.84433	.03	None Manufacturer's spec = 6.95 ± .15 V	High = +6.99383 +6.95949 Low = +6.84433	.03
T _c over range -55°C ←T _A ≤ 25°C (PPM/°C)	High = +.54 +.23 Low =18	0.2	None	High = +.59 +.23 Low =18	0.2
T _c over range 25°C≤T _A ≤ 85°C (PPM/°C)	High = +0.7 +.3 Low = +0.2	0.3	None	High = +0.7 +.3 Low = +0.2	0.3
T _C over range 85°C≰T _A ≤ 125°C (PPM/°C)	High = +7.9 -4.9 Low = -78.1	20.1	-19.7, device #1 -78.1, device #19	High = +7.9 +1.4 Low = -9.8	5.3
Heater Power dissipated at T _A = -55°C (mW)	High = 566.4 521.6 Low = 486.0	23.9	None	High = .66.4 521.6 Low = 486.0	23.9
Heater Power dissipated at TA = 25°C (mW)	High = 239.6 212.3 Low = 189.2	15.0	None	High = 239.6 212.3 Low = 189.2	15.0
Heater Power dissipation at TA = 85°C (mW)	High = 64.8 43.8 Low = 28.0	14.7	None	High = 64.8 43.8 Low = 28.0	14.7
Heater Power dissipated at T _A = 125°C (mW)	High = 33.9 30.5 Low = 26.9	2.2	None	High = 33.9 30.5 Low = 26.9	2.2

Notes: 1. I₁ = current through voltage reference.

V_s = temperature stabilizer voltage.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.15. Summary of Measurements at $I_1 = 11.3 \text{ mA}$; $V_s = 40 \text{ V}^{\frac{1}{2}}$ (LM199A)

			Parameter values not included		
<u>Parameter</u>	Overall Average	Overall	in Final Average and Final T, and associated device #	Final Average	Final
Reference Voltage at 25°C (volts)	High = +6.99938 +6.96488 Low = +6.85109	.03	None Manufacturer's spec	High = +6.99938 +6.96488 Low = +6.85109	.03
T _C over range -55°C ≤T _A ≤ 25°C (PPM/°C)	High = +9.3 +1.1 Low = +.18	2.0	+9.3, device #13	High = +1.1 +0.6 Low = +.18	0.3
T _C over range 25°C ←T _A ← 85°C (PPM/°C)	High = +6.4 +2.6 Low = -1.2	2.1	+6.0, device #5 +6.4, device #17	High = +3.8 +2.0 Low = -1.2	1.6
T _C over range 85°C ←T _A ← 125°C (PPM/°C)	High = +13.9 -3.8 Low = -35.4	11.4	-35.4, device #1 -16.6, device #2	High = +13.9 -0.3 Low = -12.3	7.3
Heater Power dissipation at TA = -55°C (mW)	High = 503.2 457.0 Low =	25.6	None	High = 503.2 457.0 Low = 411.6	25.6
Heater Power dissipation at T _A = 25°C (mW)	High = 173.6 145.8 Low = 120.4	15.0	None	High = 173.6 145.8 Low = 120.4	15.0
Heater Power dissipation at TA = 85°C (mW)	High = 61.6 45.5 Low = 34.8	8.5	.None	High = 61.6 45.5 Low = 34.8	8.5
Heater Power dissipation at TA = 125°C (mW)	High = 70.9 57.7 Low = 44.3	8.4	None	High = 70.9 57.7 Low = 44.3	8.4

Notes: 1. I_1 = current through voltage reference. V_s = temperature stabilizer voltage.

^{2.} Each block in the average column includes the high value, the computed average value and the low value for the specified parameter. VII -25

Table 7.16. Summary of Measurements at $I_1 = 1 \text{ mA}$; $V_s = 30 \text{ V} \frac{1}{\text{(LM199A)}}$

				1	
Parameter	2/ Overall Average		Parameter values not included in Final Average and Final \(\sigma\), and associated device \(\psi\)		Final
Initial Heater Current (mA)	High = 120 108.5 Low = 95	9.0	None	High = 120 108.5 Low = 95	9.0
Reference Volt- age Warm-up Stability t = 10 sec (PPM)	High = 15.2 9.05 Low = -5.6	5.4	None	High = 15.2 7.05 Low = -5.6	5.4
Reference Volt- age Warm-up Stability t = 1 min (PPM)	High = 5.07 0.35 Low = -9.74	3.8	None	High = 5.07 0.35 Low = -9.74	3.8
Reference Volt- age Warm-up Stability t = 5 min (PPM)	High = 1.3 - 2.4 Low = - 9.74	2.8	None	High = 1.3 - 2.4 Low = - 9.74	2.8
Reference Volt- age Temperature Cycling Hystere- sis (Positive Temp) (PPM)	High = 2.03 -0.57 Low = -2.4	1.29	None	High = 2.03 -0.57 Low = -2.4	1.29
Reference Volt- age Temperature Cycling Hystere- sis (Negative Temp) (PPM)	High = 1.3 -2.4 Low = -9.74	2.8	None	High = 1.3 -2.4 Low = -9.74	2.8

Notes: 1. I1 = current through voltage reference.

V_S = temperature stabilizer voltage.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.17. Electrical performance characteristics for device types 01 & 02 (See 3.4 unless otherwise specified)

Characteristics	Symbol	Conditions	Device	Limits			
	- 3			Type	Min.	Max.	Units
Reference Volt- age	VR	0.5mA ≰1R \$10mA VS=30V	T _A =25°C	01	6.800	7.100	V
		0.6mA4IR415mA	TA=25°C	02	6.70	7.20	
Reference Volt-		0.5mA LIR LOWA	TA=25°C	01_	- 9	9	mV
age change with			-55°C4TA 125°C	01	-12	12	
current	, ,	0.6mA = IR =15mA	TA=25°C	02	-14	14	
			-55 °C 4TA 4125 °C	02	-18	18	
Reference Volt-	▲VR	IR=1.0mA	-55°C TA 485°C	01	5	.5	PPM
age Temperature		Vs=30V	85°C TA 125°C	01	-10	10	°c
-		IR=1.0mA	-55°C4TA 125°C	02	-10	10	
Dynamic Imped-	$z_{\rm D}$	IR=ImA	VS=30V;TA=25°C	01	0	1	Ohms
ance		81=.3V;f=400Hz	TA=25°C	02	0	1	
Noise	NO	IR=1mA	VS=30V;TA=25°C	01	0	20	ųVrms
)	BW=10Hz to	TA=25°C	02	0	20	
		10kHz		1	1		
	}	IR=lmA	VS=30V;TA=25°C	01	0	7	γγp-p.
		BW=0.1Hz to	TA=25°C	02	0	7	
Temperature	Is	9v4v _S 440v	TA=25°C	01	2.5	14	mA
stabilizer	1	IR=OmA	TA=-55°C	01	6.6	28	1
supply					1		ł
current	1	}		1	}	}	}
Initial Tem-	ISI	9V4VS440V					1
perature		IR=emA	TA=25°C	01		200]
stabilizer	Į	1		1	1		}
supply current						l	
Reference Volt-	△ VR	IR=1mA	VS=30V	01	-10	10	
age temperature	(TEMP	-55°C+TA+125°C		02	-1	1	Vm
cycling	CYCLE)]	-		İ	1	
hysteresis				<u> </u>		<u> </u>	
Reference Volt-	△ VR	IR=1mA	VS=30V;TA=25°C	01	-20	20	PPM
age long term stability	A t	t=1000 hrs	T _A =45°C	02	-20	20	PPM

SECTION VIII

SAMPLE/HOLD CIRCUITS MIL-M-38510/125

TABLE OF CONTENTS

		Page
8.1	Background and Introduction	VIII-1
8.2	Device Type Description	VIII-1
8.3	Device Characterization	VIII-3
8.4	Discussion	VIII-3
8.5	Bibliography	VIII-3

LIST OF FIGURES AND TABLES

Figure	Title	Page
8-1	LF198 Functional Schematic	VIII-2
8-2	LF198 S/H Test Circuit	VIII-7
8-3	LF198 S/H waveforms vs hold capacitor	VIII-1
8-4	LF198 S/H waveforms vs signal level	VIII-1
Table		
8-1	Generic LF198 electrical specification	VIII-4
8-2	JC-41 Committee LF198 electrical characteristics	VIII-5
8-3	LF198 sample/hold test procedure	VIII-8

SECTION VIII

SAMPLE/HOLD CIRCUITS MIL-M-38510/125

8.1 Background and Introduction

With the advent of monolithic sample/hold circuits and their use in the expanding fields of data acquisition and data distribution, the time was right to characterize and specify these devices for military systems. National Semiconductor's LF198 was the first characterization candidate to be proposed by the JC-41 Committee. Although this report only covers the LF198, a variety of other devices may eventually be added to the future slash sheet MIL-M-38510/125.

A list of popular sample/hold circuits is shown below:

Generic Industry Typ e	Manufacturer
LF198	NSC, AMD, Signetics
SMP-11, -81	PMI
нА2420	Harris
IH5115	Intersil
LH0023, 0043, 0053	NS C

Analog Devices

At the time of this writing (October 1979) characterization work on the LF198 is only in the beginning stages. Most device parameters and test conditions have been identified. Test results, data analysis and final slash sheet recommendations will not be included in this report.

8.2 Device Type Description

AD582

The LF198 is a monolithic, unity gain, closed loop type sample/hold circuit. A functional schematic is shown in Figure 8-1. When this device is in the sample mode with the switch closed, the hold capacitor charges to whatever level it takes to make the output equal to the input. Gain accuracy of \pm .02% is guaranteed over the military temperature range with a typical acquisition time of 6 us. Bi-FET technology is used to make the J-FET input transistors of the output buffer amplifier and thus minimize the loading on the external hold

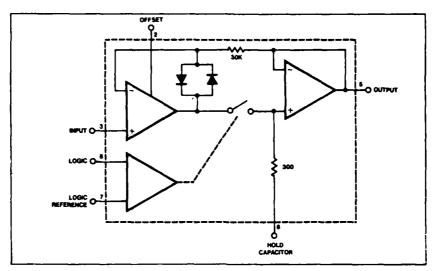


Figure 8-1. LF198 S/H functional schematic.

capacitor. Bi-polar transistors are used for the inputs of the signal amplifier to obtain low offset voltage and wide bandwidth. Unlike many hybrid and modular sample/holds, this device has an operating power supply range from \pm 5 V to \pm 18 V. Feed through in the hold mode has been minimized to 0.1 pf from input to output. Mode control is exercised through a TTL compatible differential comparator with a nominal threshold of 1.2 V. Acquisition time, droop rate, hold step and dynamic sampling error are important sample/hold parameters which are very much dependent on the hold capacitor as well as the device itself.

It is almost obvious to see that a smaller capacitor will yield a faster acquisition time and small dynamic sampling error at the expense of higher hold step and droop rate. The quality of the storage capacitor is also critical to sample/hold circuit performance. Only capacitors with low dielectric absorption will resist excessive "sag back" after being subjected to a quick charge of input voltage. Teflon, polypropylene and polystyrene capacitors have this low hysteresis feature whereas mica and ceramic types do not.

The back-to-back diodes and the 30 K ohm resistor maintain a feed back path for the input buffer when the device is in the hold mode.

Without this feature, the buffer input impedance could change as a function of being in the sample or hold mode. Also with the input buffer loop open, there would be a greater tendency for overload recovery time problems and acquisition time would be compromised.

8.3 Device Characterization

The LF198 is the first sample/hold circuit to be characterized and specified for a MIL-M-38510 slash sheet. Therefore, the commercial data sheet had to be critically examined to determine what additional parameters and test conditions, if any, would be required for an adequate military specification. Table 8-1 shows the generic LF198 electrical specifications. Further details on additional parameters and conditions to satisfy a slash sheet specification are shown in the JC-41 Committee electrical performance characteristics of Table 8-2. Next, a test procedure had to be formulated on how to measure the various sample/hold parameters.

Some very useful ideas and procedures were provided by National Semiconductor and Advanced Micro Devices. This manufacturer information was then used in developing a test circuit and a quasi Table III for the proposed MIL-M-38510/125 specification. Copies of the GEOS information were submitted to the JC-41 Committee for review and comment. The test circuit and test procedure are shown in Figure 8-2 and Table 8-3, respectively. Most of the sample/hold electrical characteristics will be measured on the S-3263 test system, automatically.

Some oscilloscope waveforms which show the relationships between the input, output and logic signals as a function of hold capacitance and signal level are shown in Figures 8-3 and 8-4.

8.4 Discussion

The LF198 characterization work will be covered completely in the next final report. At this time the device looks very promising and no major characterization problems are foreseen.

- 8.5 Bibliography
- 8.5.1 Linear Databook, National Semiconductor (1978)
- 8.5.2 C. Nelson, "I.C. Sample and Hold is 0.01% Accurate", E. E. Times I.C. Applications Conference Proceedings, 1977.
- 8.5.3 C. Nelson, National Semiconductor, LF198 Test Information (not published).
- 8.5.4 M. Mullen, Advanced Micro Devices, LF198 Test Information (not published).

absolute maximum ratings

LF198

LF298

LF398

Storage Temperature Range

Supply Voltage
Power Dissipation (Package Limitation) (Note 1)
Operating Ambient Temperature Range

1) 500 mW --55°C to +125°C --25°C to +85°C

:18V

Input Voltage Equal to Supply Voltage
Logic To Logic Reference Differential Voltage +7V, -30V
(Note 2)

-85°C to +125°C Output Short Circuit Duration
-25°C to +85°C Hold Capacitor Short Circuit Duration
0°C to +70°C Lead Temperature (Soldering, 10 seconds)

Indefinite 10 sec 300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS		LF198/LF29	8	L	- LF398		UNIT
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Input Offset Voltage, (Note 6)	Tj = 25°C Full Temperature Range		1	3 5		2	7 10	mV mV
Input Bias Current, (Note 6)	Tj = 25°C Full Temperature Range		5	25 75	}	10	50 100	nA nA
Input Impedance	T _i = 25°C		1010		1	1010		Ω
Gain Error	Tj = 25°C, R _L = 10k Full Temperature Range		0.002	0 005 0.02	i	0 004	0.01 0.02	*
Feedthrough Attenuation Ratio at 1 kHz	T _j = 25°C, C _h = 0.01μF	86	96		80	90	<u> </u>	dB
Output Impedance	, T _j = 25°C, "HOLD" mode Full Temperature Range		05	2		0.5	4 6	Ω
"HOLD" Step, (Note 4)	Tj = 25°C, Ch = 0.01µF, VOUT = 0		0.5	20	ļ	10	2 5	m۷
Supply Current, (Note 6)	τ _j ≥ 25°C		4.5	5.5	ļ	4.5	6.5	mA.
Logic and Logic Reference Input	τ _j = 25°C		2	10		2	10	μΑ
Leakage Current into Hold Capacitor (Note 6)	T _j = 25°C, (Note 5) Hold Mode		30	100		30	200	₽Ā
Acquisition Time to 0.1%	ΔV _{OUT} = 10V, C _h = 1000 ρF C _h = 0.01μF	ı	4 20			4 20		μs μ1
Hold Capacitor Charging Current	VIN - VOUT # 2V		5		1	5		mA
Supply Voltage Rejection Ratio	V _{OUT} ±0 .	80	110		80	110	ĺ	₫B
Differential Logic Threshold	T _i = 25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198 is 150°C, for the LF298, 115°C, and for the LF398, 100°C. When operating at elevated ambient temperature, the TO-5 package must be denated based on a thermal resistance (9jA) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

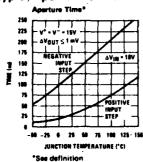
Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25^{\circ}C$, $-11.5V \le V_{IN} \le \pm 11.5V$, $C_h = 0.01 \mu F$, and $R_L = 10 \ k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

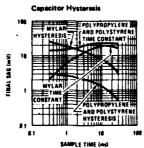
Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01 µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters guaranteed over a supply voltage range of ±5 to ±18V.

typical performance characteristics





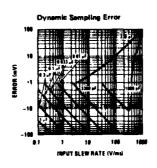


Table 8-1. Generic LF198 electrical specification.

LF 198 ELECTRICAL PERFORMANCE CHARACTERISTICS

Unless otherwise	specif:	specified the device is in the sample mode			•
TA = - 55°C to +	125°C,	$V_s + 15$, $V_{in} - 11.5$ to + 11.5 V, $C_h = .01$ uf		Limits	
Characteristic	Symbol	Conditions	Min	Max	Units
Input Offset	VTO	$V_S \pm 5V \text{ to } \pm 15V \text{ V}_{1n} = 0V$ $T_A = 25^{\circ}\text{ C}$	-3	+3	À
Voltage	2	-55°C & TA & + 125°C	5	+5	Λm
Input Bias		$T_{A} = 25^{\circ} C$	-1	25	Æ
Current	IIB		-75	75	¥
Input	t	$T_A = 25^{\circ}C$	2	1	4
Impedance	7 .1		1		40
Gain			005	+.005	%
Error	Ae	$V_{in}=0$ to -11.5V, $V_{in}=0$ to +11.5V, $R_{L}=10R$	02	+.02	12
Gain		$V_{S}=\pm 5V$ $T_{A} = 25^{\circ}C$	02	+.02	12
Error	Ae	$V_{in}=0$ to $-2V$, $V_{in}=0$ to $+2V$, $R_L=10K$	04	+.04	100
Feedthrough		$V_{out} = -11.5V$, +11.5V $T_A = 25^{\circ}C$	98	•	фВ
Attenuator Ratio	FRR1	Vin= ±15C Ch= .0luf DC Test, Hold Made	08	-	dВ
Feedthrough		$T_A = 25^{\circ}C$			
Attenuator Ratio at 1 kHz	FRR2	Vin= 10 Vpp Vout=0V, Ch= .01 uf	98	1	dB.
Output		Hold Mode Ch=ÛV	-	7	4
Impedance	Zout	Vout=0V, $I_0=\pm 1mA$, $V_{in}=0V$ $T_A=25^{\circ}C$	•	2	વ
"Ho1d"			-5	5	
Step	Vhs	$V_{1g} = 0$ to 4V, T_r 50 ns $V_{out} = \pm 11.5$ V $T_A = 25^{\circ}$ C	-2	2	
Supply	ŀ	9	_	5*9	A.
Currenc	TCC	V_S = 16V Sample Mode +25°C \leq T _A \leq 125°C	-	5*5	H.
Logic Input	IIH,		-10	+10	ηΨ
Current	$_{ m II}$	$V_{1n}=0V V_{L}=0V, V_{LR}=5.5V; V_{L}=5.5V V_{LR}=0V$	-20	+20	A II

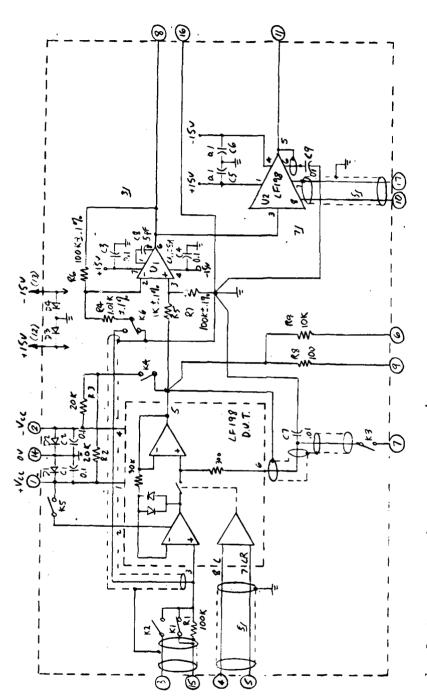
TABLE 8-2. JC-41 Committee LF198 electrical performance characteristics.

Au Au

ELECTRICAL PERFORMANCE CHARACTERISTICS (cont.)

ľ				Limits	
Characteristic	Symbol	Conditions	Min	Max	Units
Hold Mode Leakage Current	$ m I_L$	V_{out} ± 11.5 V_{out} T _J = 25°C	-100	100	pA
Hold Mode Leakage Current	$T_{ m I}$	V _{out} = ± 11.5V -55°C ≤ T _J ≤ 125°C	-100	100	Ψu
Hold Cap Charge Current	Ich	$V_{in} - V_{out} = 2V V_{out} = \pm 11.5V T_A = 25^{\circ}C$	3		¥E €
Power Supply Rejection Ratio	+PSRR	$+12 \text{ to } +18V, V_{in} = 0$	80		dB
Power Supply Rejection Ratio	-PSRR	$V+ = 18V$, $V- = -12$ to $-18V$, $V_{in} = 0$.08		dB
Diff Logic Threshold	Vth	$V_{LR} = 0V$, $V_{in} = 0V$	0.8	2.0	>
Acquisition Time to .01%	taq	$V_{in} = 0$ to + 10V $CL = 100$ uf $V_{in} = 0$ to - 10V $Ch = .01$ uf $T_{A} = 25^{\circ}C$	•	25	sn
Noise	en	10 to 100 K Hold mode, sample mode $T_{\rm A}=25^{\circ}{\rm C}$		25	uVaV
Hold Mode Set- tling Time	ts	0 to 10 V input Vin = 0 , Vout < 1 mV $_{ m IA}$ = 25°C	1	1.5	sn
Aperture Time	tap	Ch = .01, $V_{out} \le 1 \text{ mV}$ $V_{in} = 10 \text{V}$ $T_{A} = 25 ^{\circ} \text{C}$	•	200	su

TABLE 8-2. JC-41 Committee LF198 electrical performance characteristics.



Last component designations are R9, C9, U2, D4 and K6. All resistors are \pm 1% film unless otherwise stated. Notes:

This error shall be removed in ${
m Ul}$ offset error shall be measured with pin 9 grounded. the software calculations.

Relay control inputs are not shown.

A speed up circuit is required in series with the logic input for rise times greater

Circled pin numbers are top socket connections. All other pins are undersocket connections. The adapter S/H U2 is required for $ext{T}_{A}$ =125°C testing of some parameters. 6.

LF198 S/H test circuit. Figure 8-2.

TABLE III. Group & inspection for all device types

		ite Equation 2/ Min Nax Units	# 10 gl	10 62	VIO = 10 E4		+IIB = 100 (E6-E1) 1 25 CA +ITE = 100 (F7-F2)	28	Z1 = 0.23/(E1+E7-E2-E6) 2 - G	005 .005	AE = (E11-E12)/40202		VIO (ADJ) = 10 (E3-E13) 10 - mV	+PSRR = 20 log [600/(E14-E15)] 80 - dB	-PSRR = 20 log 600/(E14-E16)	11500/0818-1171	= 20 log (1500/(E19-E18))	# 20 log	Zo = 5 (E23 -E22) - 2 A	VHS = 10 (E25-E24) - 2 2 mV	V _{HS} = 10 (R27-E26)	I.c. 11	IH 12 0 10	·
nevice che	Measured Pin	No Value Units	9 81 V	2 22	428		8 22 2 23	82 4	-	8 E9 V	E11	B12	E13	. E14 E15	E16	1817	E18	E21	E22 E23	824 825	E26	2 I1 M	4 12 uA	
	Dergized	Ц	None	_		1	<u>-</u>	•	2 puis	3		• ;	Q	None	•	к1, к2			K3	, K6		None		
	Mumbers (see Fig. 7)	5 6 6 7	-11.5V Open Open	8	-2v	11 Sv		0 v	tests 1,2,6,	11.5V Open Open	-2v	i i	\$ +						-10 v 0v 10 v 0v	10-11.5v Open Open	11.50	g-	5.5v	
	Adapter Pin Mu		26.5VOpen - 9V		74 0.54	$\overline{}$	147	-15v 🕴 2.5v	Calculate using data from	Open - 9v	0.5v	2 54	-	-18v -18v	1Z1	-Ly See Fig. 8	Ciming waveforms	>	See Fig. 9	-26.5V See Fig. 10	-3.5v	-15V Open 2.5V	21.5v 5.5v	_
	Kotes	~		15 V	> > 6	3.54.2		15 V -1	Calcula	3.5V-26.5V 26.5V- 3.5V	3 0	47	. T	18 V -1 12 V -1	18 A P.	4/, 15 V -P			<u>5/</u>	3.5v	$\frac{6}{2}$, $\frac{26.5}{1}$	15v -1		20
4	Test	7	<u> </u>	m'4	* vn	۰	~	œ	6	8:	212	1 2		15	16	17	1 19	20	21 .	22	23	24	28.23	
M71.488	Symbol	-	V ₁₀ 4001			±I,I	· ·	>	21	N N	,	To (ADJ.)	- 1	+PSRR 4003	-PSRR .	FRR			20	VIES		301	П	-
	Subgroup	(2)	1,2,3				_						_						-					

Table 8-3. LF198 sample/hold test procedure.

TABLE III. Group A inspection for all device types

		Units	a -	ă	\top	> 8	+	1	a z	uV/°C	3			9 11	_	_	3-	- 5	a	14	W.
	٠ •	Yex	۶ .	8 -		- 7			-	2	25			8			2				25
Ì	@ 25°C	Hin	-30	-100		4.		-	7	-20	1.	_		-		_	1.	88	†	1	
		Equation	los (+) = 16 los (-) = 17	(E29 - E28)	IHL(-) = 100 (E31 - E30)	I _{CH} (+) = 18	1 (-) HOI	Vru(B) < 2.00 1f 150 > 1 II	12	\dagger		tac = t2 tac = t3			tap = t6	tap = t8	te = t9 te = t10	FRREC = 20 log 2000/E41	IR(tr) = tl (see Fig. 16)	IR(0s) = 100 (Av01/v01)	NI (BB) = E42/100 NI (BB) = E43/100
,	Pfa	Unite	≨ -	> -		> ≦	+	1	돌		3	_	_	a		-	9	dás	2	}~ →	uVrms
	Heasured Pin	Value	91	£28 £29	E30	9 <u>2</u>	61	110	Ē		2	ខ្លួ	2	2	t2	2	£ 20	173	=	,01, V01	E42 E43
$\ $	£	£	6-7		-	-	\vdash		-	25.03	∞-							-		,	•
	Energized	Relays	к1, к2	None		K1,K2,K3	_		>	25°C & OCH)/ (T	к1,к2,к6					•	None				
	18. 7)	7	Open			9.5V	. 5v	8	•		Open		_								-
	(See F	٥	oben -		_			_	-	- V ₁₀ @	Open										
	umbers	2	8-	-11.5v	, S. →	8.			ŀ	ğ	8-										
	Adapter Pin Numbers (See Fig. 7)	2 3 4	10v 2.5v	.5\See Fig. 11 timing	'	/ 11.5v 2.5v	-11. Sv	- 2v 2.0v	- 2V 0.8V	- (V _{IO} @T&		vaveforms	flow chart	See Fig. 13	waveforms	flow.chart	See Fig. 14	20VPP 0V	50mV 2.5V	→	0v 2.5v Dv
1.		-	15v - 15v	3.5v -26.5v	3.50	-15v			1	AVIO/AT	15%			_	-						
1	اـ	7			26.39	150				٨	15v								-		
ļ	Noce	4	9۱	/ <u>or</u>) Pl	司	Ħ	12/	/21		<u>=</u>			/77	, -	_	沟	/91	킈	_	
	7	ė	8 8	31	22	33	*	35	36	3	88	3 3 3	‡	42	43		46	87	\$	2	2 22
VII - 04'B	-883	Method	3011															:	,		
	Symbol		Ios (+) Ios (-)	1HL (+)	I _{HL} (-)	I _{CH} (+)	ICH(•)	VTH(H)	VTH(L)	AV10/AT	t a c			t≜p			:	FRRAC	TR(tr)	I K(GB)	NI (BB)
	Subgroup Symbol	T	1,2,3	·	•				ļ	1,2,3	4						21	^			

Table 8-3. LF198 sample/hold test procedure (cont'd).

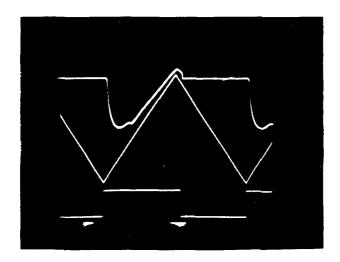
LF198 Sample/Hold Test Procedure Notes

- 1/ In order to remove test amplifier offset from the data values measure the offset of Ul on pin 8 with pin 9 grounded.
 - Software subtraction techniques should be used to correct the data.
- 2/ The equations take into account the test amplifier gain of 100 and other circuit constants so that the calculated value is in Table I units.
- 3/ Common mode input range conditions are exercised by grounding the signal input and swinging the power supplies to their nominal levels minus the common mode voltage. For example for $V_{CM} = +11.5 \text{ V}$, $+ V_{CC} = 15 \text{ V} 11.5 = 3.5$ and $V_{CC} = -15 \text{ V} 11.5 \text{ V} = -26.5 \text{ V}$.
- 4/ With a 0 V signal input the D.U.T. logic input is switched from 2.5 V to 0 V. This resets the system in the hold mode. The test amplifier output is measured immediately after each 15 V change at the signal input.
- 5/ E22 and E23 are measured with the D.U.T. in the hold mode.
- 6/ For the hold step test, the first and second measurements are made with the D.U.T. in the sample and hold modes respectively.
- 7/ Logic input step changes should have a rise time of 0.5 u seconds or less.
- 8/ High and low state logic input currents shall be measured over the common mode voltage range as shown.
- 9/ The output shall be shorted to ground for 25 milliseconds or less.
- 10/ Hold leakage current at 25°C is determined by measuring the droop referred to the test amplifier output over a one second interval.
- 11/ The charge current measurements on pin 7 is referenced to forced voltages of 9.5 V and 9.5 V respectively.
- 12/ With worst case logic threshold voltages applied, the hold cap terminal output current is measured to determine if the device is in the correct operating mode.
- 13/ Step the signal input from 0 V to + 10 V. After a delay of ≈ 100 usec generate a 100 usec sample mode pulse. The difference between the input and D.U.T. output is monitored with a high differential amplifier. Reduce the sample mode pulse width until there is a 10 mV (0.1%) change from the 100 usec pulse value. The sample mode pulse width for this condition is the acquisition time. Repeat the above procedure for input signal transitions of 10 V to 0 V, 0 V to 10 V and 10 V to 0 V. Figure 12 shows an automatic flow chart method and a simplified manual method for determining acquisition time.

Table 8-3. LF198 sample/hold test procedure (cont.).

- 14/ Step the logic input from 5 V to 0 V with the input at 0 V. After a 2 usec time delay step the signal input up to 10 V. For this condition the D.U.T. output should be 2 0 V. Gradually decrease the delay until a 10 mV (.1%) shift occurs at the D.U.T. output. Repeat the above procedure for input signal transitions of 10 V to 0 V, 0 V to 10 V and 10 V to 0 V. The delay corresponding to the 10 mV shift is equal to the aperture time.
- 15/ Settling time is determined by adding the aperture time to the additional increment of time during which the output in the hold mode is greater than one millivolt from final value.
- Dynamic feedthrough rejection is determined in the hold mode with a signal input of 20 Vpp at a frequency of 1 kHz.
- 17/ Overshoot TR (OS) and rise time TR (tr) are indicative of the stability and bandwidth of the device, respectively.
- 18/ Broadband noise NI (BB) of the D.U.T. is extracted from the total noise of the D.U.T. and a low noise op amp such as the SE5534.

Table 8-3. LF198 sample/hold test procedure (cont.)



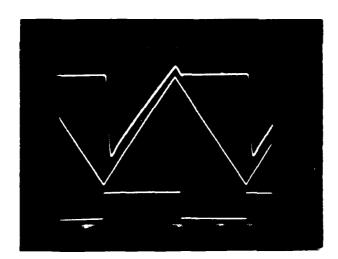
 v_{out} @ 5 v/div.

V_{in} @ 5 V/div. (Triangle Freq = 30 kHz)

 $\rm v_{LOG}$ @ 2 $\rm V/div.$

Time @ 5 usec/div.

 $C_{\text{HOLD}} = 0.01 \text{ uF}$



V_{out} @ 5 V/div.

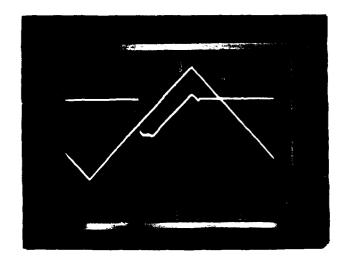
V_{in} @ 5 V/div. (Triangle Freq = 30 kHz)

 v_{LOG} @ 2 v/div.

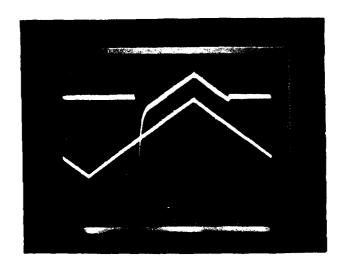
Time @ 5 usec/div.

 $C_{\text{HOLD}} = 0.001 \text{ uF}$

Figure 8-3. LF198 sample/hold waveforms vs. hold capacitor.



Vout @ 5 V/div.
Vin @ 5 V/div.
Time @ 10 us/div.
C = .01 uF



V_{out} @ 50 mV/div.
V_{in} @ 50 mV/div.
Time @ 10 us/div.
C = .01 uF

Figure 8-4. LF198 sample/hold waveforms vs. signal level.

SECTION IX

VOLTAGE REGULATORS, NEGATIVE

MIL-M-38510/115

TABLE OF CONTENTS

		Page
	List of Figures	IX-ii
9.1	Background and Introduction	IX-1
9.2	Start-up Investigations and Results	IX-1
9.3	Conclusions	1x-3

		Page
	List of Figures	IX-4
9.1	Manually Controlled Start-up Voltage Circuit	
9.2	Solid State Controlled Start-up and Recovery Voltage Circuit	IX-5

SECTION IX

VOLTAGE REGULATORS, NEGATIVE

MIL-M-38510/115

9.1 Background and Introduction

The characterization effort of fixed negative voltage regulators was undertaken in 1978 and is reported in RADC-TR-78-275 Final Technical Report. The report noted observations that indicated several device anomalies, such as; a) start-up and output short circuit current problems under different input voltages and load currents, b) emitter-follower type oscillations and c) hot-socket insertion/extraction failures. Emitter-follower type oscillations and hot-socket insertion/extraction failures were investigated and solutions to these problems were presented. Information relation to problems of this type may be found in an article "Designer's Guide to: I.C. Voltage Regulators" by Robert Dobkin published in EDN August 20, 1979 and September 5, 1979. The start-up anomaly was observed immediately prior to the writing of the above mentioned report. Investigations were continued after the report was issued for publication and are presented herein.

9.2 Start-up Investigations and Results

The investigation of the start-up problem was initiated as a result of comments made at a JC-41 Committee meeting in March of 1978. At this meeting various members disclosed that some regulators failed to start or were specified in such a way that devices that would not start would not be detected. The investigation at OS began with the construction of the test circuit shown in Figure 9.1. The switch, 3-1, was connected to a stiff high current power supply and the test was performed under various load conditions. The test was performed repeatedly and occasional failures were observed by three individuals at OS test facilities. As simple as this test appeared, it had the drawback that the on/off duty cycle, for power to the device, was uncontrolled; and, since these devices are tested without a heat sink, it is quite possible that with this over-simplified test circuit they were driven into their thermal shut-down mode.

In order to eliminate the suspected thermal shut down problem, a special solid state start-up circuit was constructed and is shown in its final form in Figure 9.2. This circuit was used to test devices that had previously failed start-up at OS, but could not be confirmed at the manufacturer's test facility. The use of relays for this test was rejected because it was felt that relay chatter would introduce an uncontrolled test condition. The pass transistor, used in the circuit in

Figure 9.2, is a power darlington transistor and can provide sufficiently high initial current for the start-up test. A current regulator is used in the base of the power darlington, and the current into the base of the transistor is regulated by the op amp and the shunt transistor to ground. Because of the high capacitive load circuit at the power darlington emitter and the high impedance input circuit at the power darlington base, it was necessary to add stabilizing capacitors to the control circuit in order to eliminate emitter-follower oscillations. The closed loop gain of the start-up circuit has a gain of 10 so that voltages as high as 40 can be easily programmed by either an automatic tester or a pulse generator. With this start-up circuit, the duty cycle of the regulator on-time was set for 2%. No start up failures were observed on the oscilloscope; so, the duty cycle was increased. As the duty cycle increased, intermittent start-up problems were observed. This circuit confirmed the suspicion that the initial observation was due to uncontrolled heating of the device which went into thermal shut-down.

At a later meeting of the JC-41 Committee, it was learned that the start-up problem could occur if the regulator output was momentarily shorted to ground. To test this parameter the circuit, shown in Figure 9.2, at the output of the regulator was developed. With this circuit, the output is forced to zero volts. The forcing voltage is then removed and the device is allowed to recover into a resistive capacitive load. OS recommends that this anomaly be called voltage recovery. Both start-up and voltage recovery tests are discussed in Section 3.

Some negative voltage regulators with date code 7619 and 7639 were tested in this test circuit. The devices all started-up at 25°C with input voltages between - 30V and -8 Volts and with load conditions in accordance with the test specification. However, with the input voltage magnitude greater than 25 volts and the case temperature greater than 60°C, a few of these regulators failed to recover with the specified load current. Negative regulators with date codes 78XX were also tested and passed the voltage recovery test with a case temperature of 125°C.

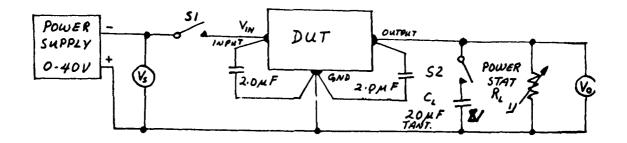
Additional testing on the 76XX data code devices that failed the voltage recovery test revealed that the input-to-output voltage differential is very critical. For case temperatures above 60°C and with a specified load condition, these devices shut down when the input-to-output voltage magnitude was greater than 20 volts. None of the tested negative voltage regulators, with date codes 78XX, showed this anomaly.

9.3 Conclusions

Start-up problems originally identified by GEOS in 1978 apparently were due to the use of an uncontrolled ON-time duty cycle of the regulator, causing random thermal shutdown to occur. Present testing indicates that start-up problems do not exist with any regulators specified in MIL-M-38510/115, /117, /118.

Voltage recovery problems may exist with devices from one vendor, having date codes prior to 1978. Devices qualified to MIL-M-38510 will not exhibit voltage recovery problems, which have been designed out by the vendor in question.

Hot socket & emitter follower oscillations were resolved in the aforementioned report. The findings and resolutions for these anomalies are still valid.



Device Type	01	02	03	04	05	06	07	08	Test Condition Group
R. for IL= SmA	1.0Kn	2.4Kn	3.0Kn	4.8Kn	1.0Km	2.4Kn	3.0K-2	4.8Ka	:
Vin (min)	8 Vde	15 Vde	18.5Vd	28 Vde	8 Vdc	15 Vdc	18.5 Vdc	28 Vdc	1
VIN (max)	35 Vdc	35 Vdc	35 Valc	40Vde	3 <i>5 Vd</i> k	35 Vdc	35 Kdc	40 Vdc	
Rifor I = 350mA500m	14.3s	34.2	43 A	68 A	102	242	302	48 s	
1 Vin (min)						15 Vde			2
[VIN (max)]	25 Vde	32Vdc	35Vdc	40Vdc	25 Vdc	32 Vdc	35 Vdc	40Vde	
R_L for $I_L = I_L(max)$	10a	245	30.a	48_s	51	121	15_2	242	_
IVIN (min)	8 Vdc	15 Vde	18.5 Vde	28 Vdc	8 Vdc	15 Vde	18.514	28 Vde	3
[Vin (max)]	20Vdc	27 Vdc	30 Vde	38 Vdc	201de	27Vde	30 Vdc	38 Vdc	

NOTES:

- 1/ For each device type, adjust R_L for a typical load current of 5 mA.
- 2/ Adjust $V_8 = -|V_{in}(min)|$ for the device type under test. Close switch S1 and observe that the proper voltage is at V_0 . Open S1.
- 3/ Repeat the conditions defined in 1/ and 2/ with $V_8 = -|V_{in}(max)|$ for each device type under test.
- 4/ For each device type, adjust R_L for a load current of 350 mA or 500 mA per Group 2.
- $\frac{5}{}$ Repeat the conditions defined in $\frac{2}{}$ and $\frac{3}{}$ with the load current conditions defined in $\frac{4}{}$.
- 6/ For each device type, adjust RL for a typical maximum load current.
- 7/ Repeat the conditions defined in 2/ and 3/ with the load current conditions defined in 6/.
- 8/ With S2 closed, repeat the conditions defined in 1/ through 7/.
 Figure 9.1. Manually controlled start-up test circuit.

Figure 9.2. Solid-state controlled start-up and recovery voltage circuit.

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